Dual Independent Differential Amp for Low Power Applications from DC to 120MHz

The CA3054 consists of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300MHz. These feature make the CA3054 useful from DC to 120MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

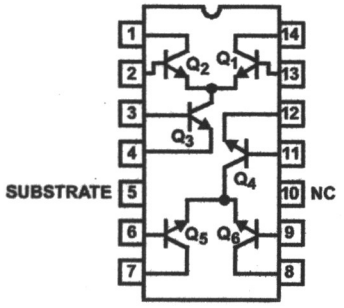
The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3054	0 to 85	14 Ld PDIP	E14.3
CA3054M96 (3054)	0 to 85	14 Ld SOIC Tape and Reel	M14.15

Pinout

CA3054
(PDIP, SOIC)
TOP VIEW



Features

- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Maximum Input Offset Voltage . . . . . ±5mV
- Temperature Range . . . . . 0^oC to 85^oC

Applications

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations
  - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

Absolute Maximum Ratings $T_A = 25^oC$

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA

Operating Conditions

Temperature Range ..... 0^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	130
SOIC Package	140

Maximum Junction Temperature (Die) ..... 175^oC
Maximum Junction Temperature (Plastic Package) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)
Maximum Power Dissipation (Any One Transistor) 300mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3054 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical Terminal 2 with respect to Terminal 4 is +15V to -5V.

(NOTE 4) TERM NO.	13	14	1	2	3	4	6	7	8	9	11	12	5
13		0, -20	Note 3	+5, -5	Note 3	+15, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
14			Note 3	Note 3	Note 3	+20, 0	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	+20, 0
1				+20, 0	Note 3	+20, 0	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	+20, 0
2					Note 3	+15, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
3						+1, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
4							Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
6								0, -20	Note 3	+5, -5	Note 3	+15, -5	Note 3
7									Note 3	Note 3	Note 3	Note 3	+20, 0
8										+20, 0	Note 3	Note 3	+20, 0
9											Note 3	+15, -5	Note 3
11												-1, -5	Note 3
12													Note 3
5													Ref. Sub-strate

Maximum Current Ratings

(NOTE 4) TERM NO.	I_{IN} mA	I_{OUT} mA
13	5	0.1
14	50	0.1
1	50	0.1
2	5	0.1
3	5	0.1
4	0.1	50
6	5	0.1
7	50	0.1
8	50	0.1
9	5	0.1
11	5	0.1
12	0.1	50

NOTES:

3. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.
4. Terminal No. 10 of CA3054 is not used.

Electrical Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS For Each Differential Amplifier						
Input Offset Voltage (Figure 8)	V_{IO}	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.45	5	mV
Input Offset Current (Figure 9)	I_{IO}	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.3	2	µA
Input Bias Current (Figure 5)	I_I	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	10	24	µA
Quiescent Operating Current Ratio (Figure 5)	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.98 to 1.02	-	-
Temperature Coefficient Magnitude of Input Offset Voltage (Figure 7)	$\frlvert\frac{\Delta V_{IO}}{\Delta T}\frrvert$	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	1.1	-	µV/°C

Electrical Specifications $T_A = 25^oC$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
FOR EACH TRANSISTOR							
DC Forward Base-to-Emitter Voltage (Figure 8)	V_{BE}	V_{CB} = 3V	I_C = 50µA	-	0.630	0.700	V
			I_C = 1mA	-	0.715	0.800	V
			I_C = 3mA	-	0.750	0.850	V
			I_C = 10mA	-	0.800	0.900	V
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3V, I_C = 1mA		-	-1.9	-	µV/°C
Collector Cutoff Current (Figure 4)	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E = 0		20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10µA, I_{CI} = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0		5	7	-	V
DYNAMIC CHARACTERISTICS							
Common Mode Rejection Ratio for each Amplifier (Figures 1, 10)	CMRR	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	100	-	dB
AGC Range, One Stage (Figures 2, 11)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	75	-	dB
Voltage Gain, Single Stage Double-Ended Output (Figures 2, 11)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	32	-	dB
AGC Range, Two Stage (Figures 3, 12)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	105	-	dB
Voltage Gain, Two Stage Double-Ended Output (Figures 3, 12)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	60	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics (For Single Transistor)							
Forward Current Transfer Ratio (Figure 13)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	110	-	-
Short Circuit Input Impedance (Figure 13)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 13)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	15.6	-	µS
Open Circuit Reverse Voltage Transfer Ratio (Figure 13)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	1.8×10^{-4}	-	-
1/f Noise Figure for Single Transistor	NF	f = 1kHz, V_{CE} = 3V		-	3.25	-	dB
Gain Bandwidth Product for Single Transistor (Figure 14)	f_T	V_{CE} = 3V, I_C = 3mA		-	550	-	MHz
Admittance Characteristics; Differential Circuit Configuration (For Each Amplifier)							
Forward Transfer Admittance (Figure 15)	Y_{21}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	-20 + j0	-	mS
Input Admittance (Figure 16)	Y_{11}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	0.22 + j0.1	-	mS
Output Admittance (Figure 17)	Y_{22}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	0.01 + j0	-	mS
Reverse Transfer Admittance (Figure 18)	Y_{12}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	-0.003 + j0	-	mS

Electrical Specifications $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Admittance Characteristics; Cascode Circuit Configuration (For Each Amplifier)						
Forward Transfer Admittance (Figure 19)	Y_{21}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	68 - j0	-	mS
Input Admittance (Figure 20)	Y_{11}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0.55 + j0	-	mS
Output Admittance (Figure 21)	Y_{22}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0 + j0.02	-	mS
Reverse Transfer Admittance (Figure 22)	Y_{12}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0.004 - j0.005	-	µS
Noise Figure	NF	f = 100MHz	-	8	-	dB

Test Circuits

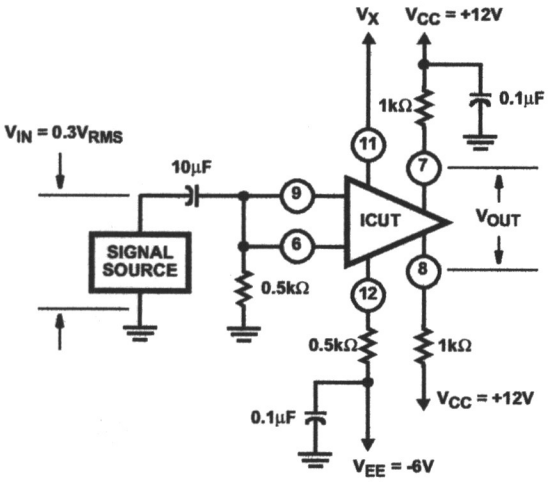


FIGURE 1. COMMON MODE REJECTION RATIO TEST SETUP

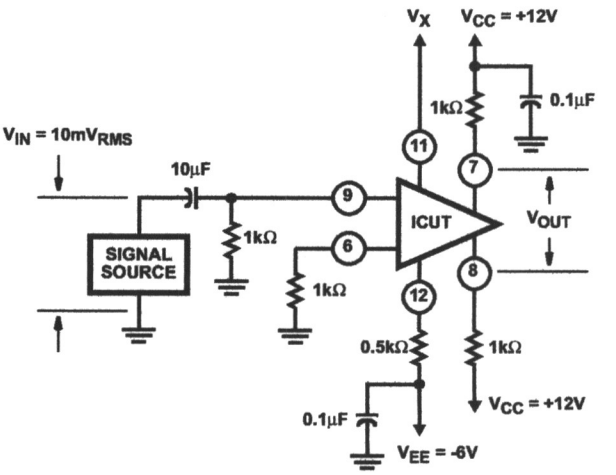


FIGURE 2. SINGLE STAGE VOLTAGE GAIN TEST SETUP

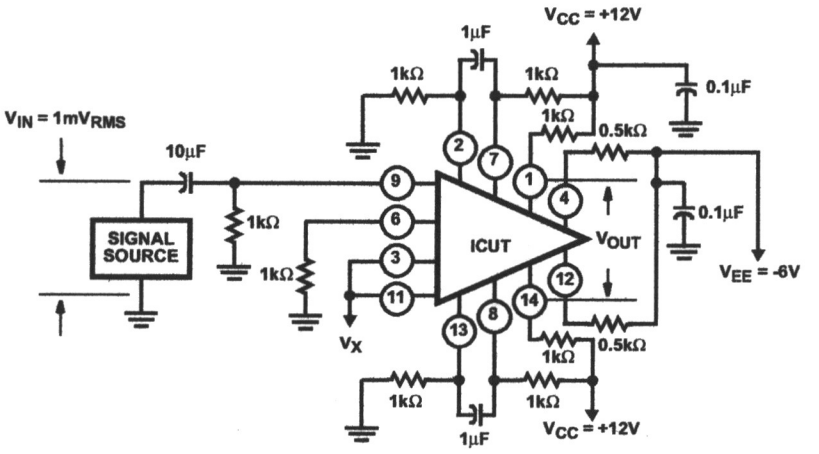
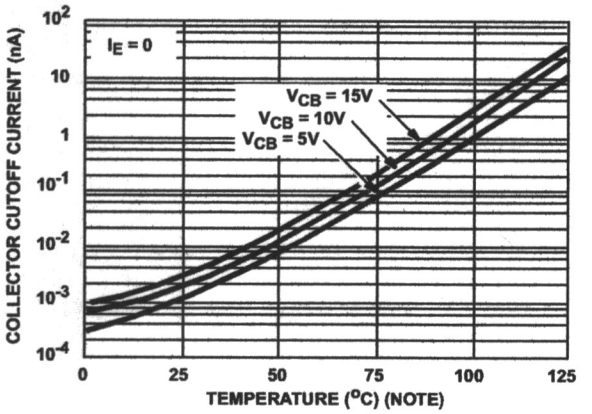


FIGURE 3. TWO STAGE VOLTAGE GAIN TEST SETUP

Typical Performance Curves



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 4. COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

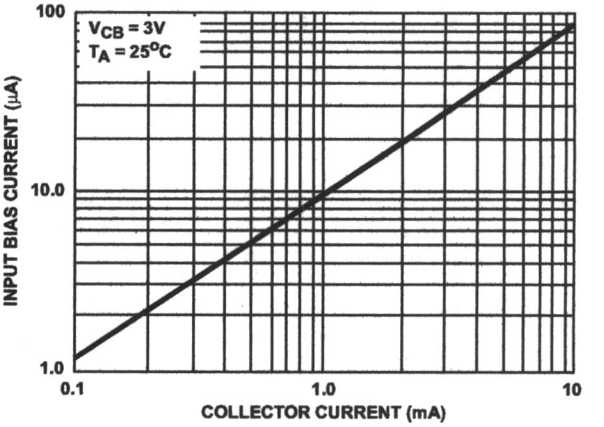
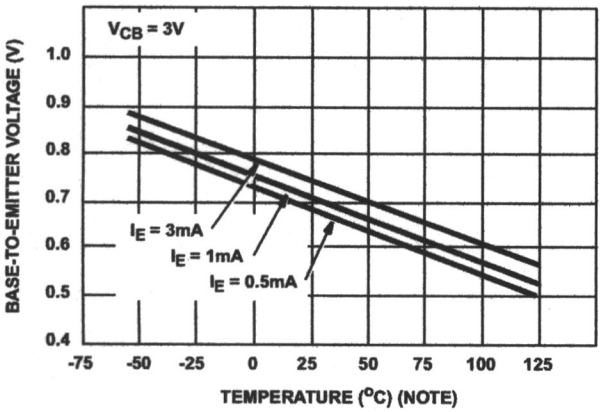
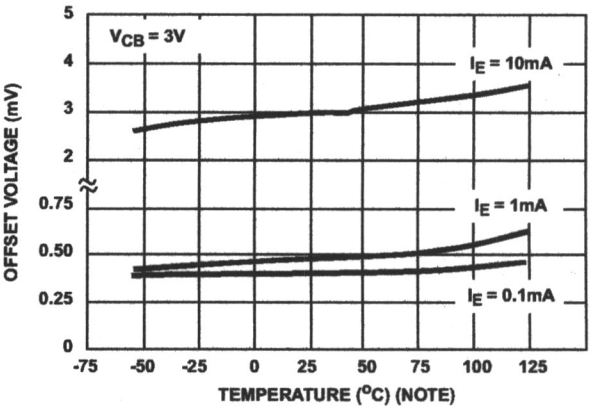


FIGURE 5. INPUT BIAS CURRENT vs COLLECTOR CURRENT FOR EACH TRANSISTOR



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 6. BASE-TO-EMITTER VOLTAGE FOR EACH TRANSISTOR vs TEMPERATURE



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE FOR DIFFERENTIAL PAIRS

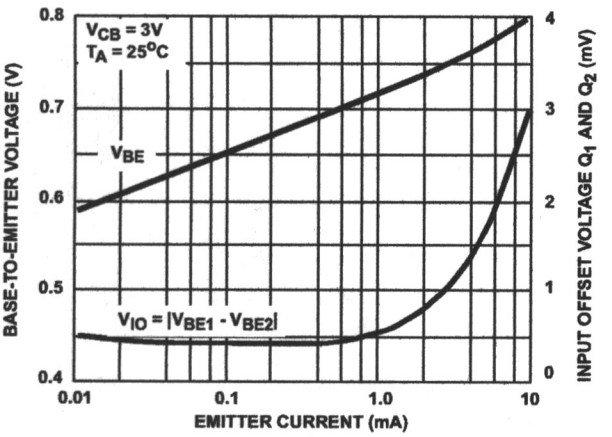


FIGURE 8. STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS vs EMITTER CURRENT

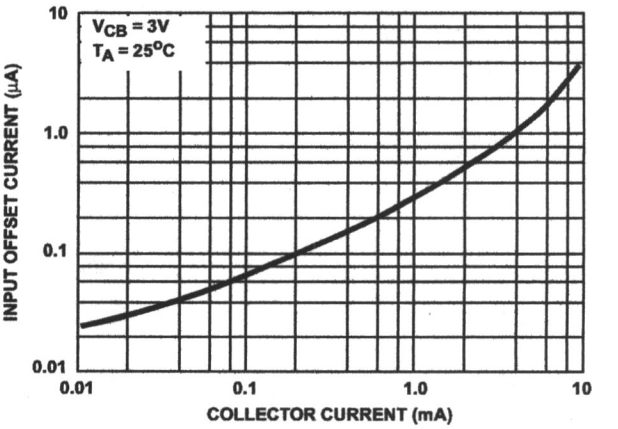


FIGURE 9. INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

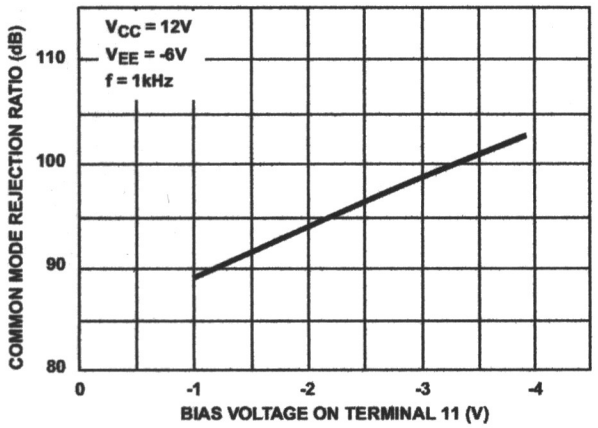


FIGURE 10. COMMON MODE REJECTION RATIO CHARACTERISTIC

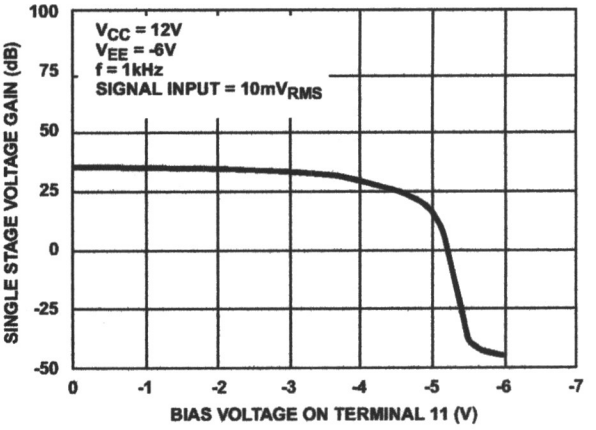


FIGURE 11. SINGLE STAGE VOLTAGE GAIN CHARACTERISTIC

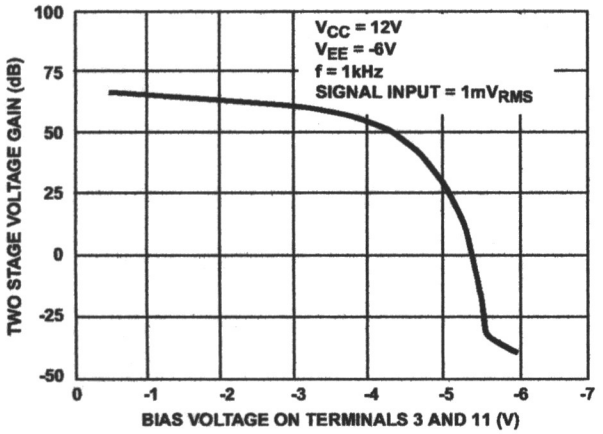


FIGURE 12. TWO STAGE VOLTAGE GAIN CHARACTERISTIC

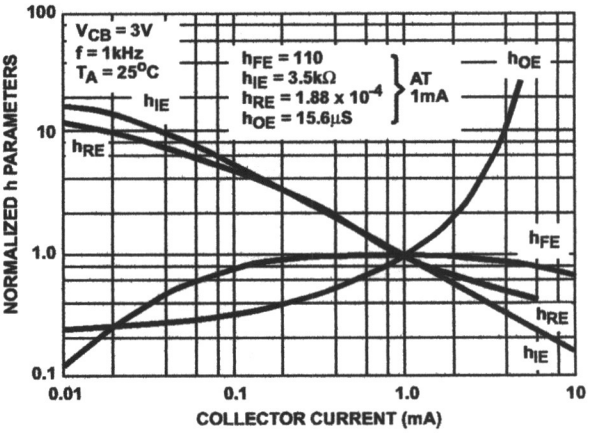


FIGURE 13. FORWARD CURRENT TRANSFER RATIO (h_{FE}), SHORT CIRCUIT INPUT IMPEDANCE (h_{IE}), OPEN CIRCUIT OUTPUT IMPEDANCE (h_{OE}), AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO (h_{RE}) vs COLLECTOR CURRENT FOR EACH TRANSISTOR

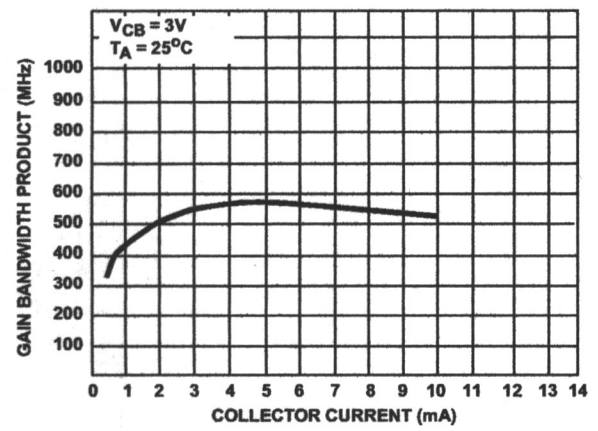


FIGURE 14. GAIN BANDWIDTH PRODUCT (f_T) vs COLLECTOR CURRENT

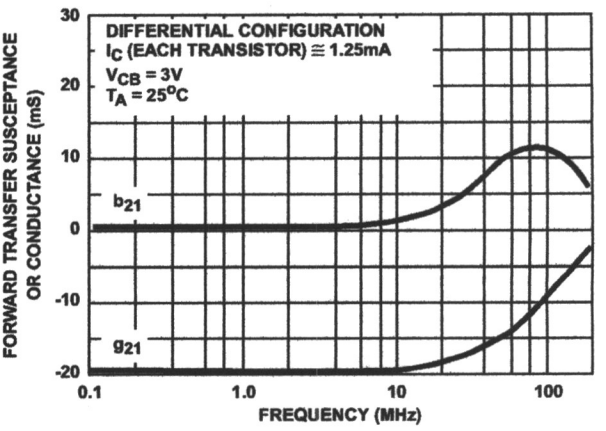


FIGURE 15. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

Typical Performance Curves (Continued)

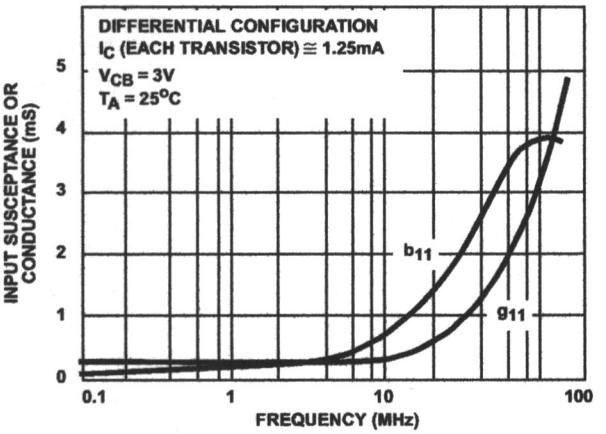


FIGURE 16. INPUT ADMITTANCE (Y_{11})

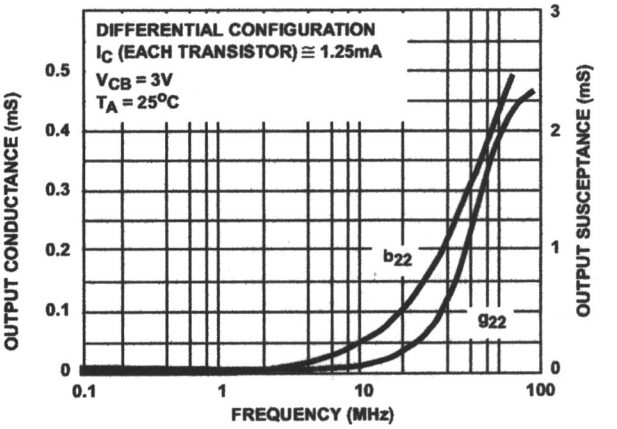


FIGURE 17. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

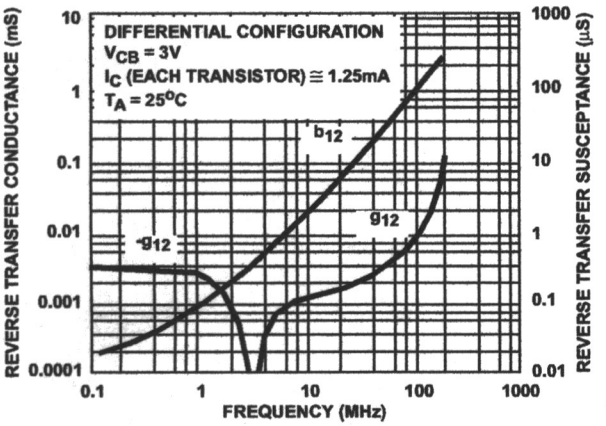


FIGURE 18. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY

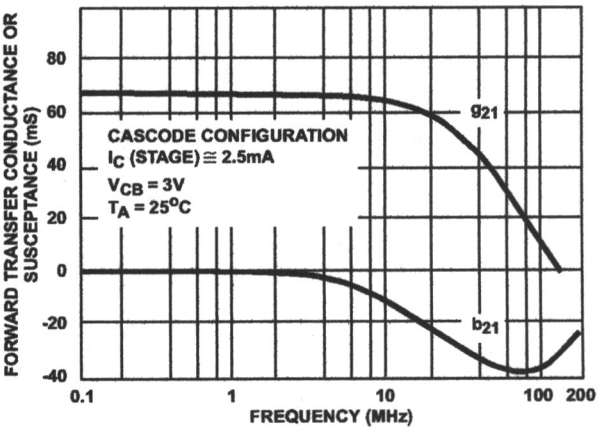


FIGURE 19. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

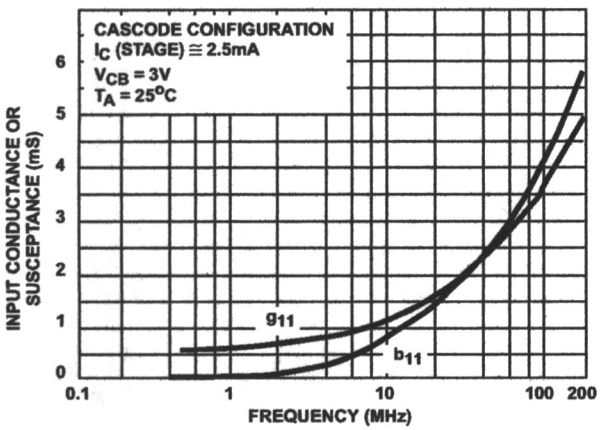


FIGURE 20. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

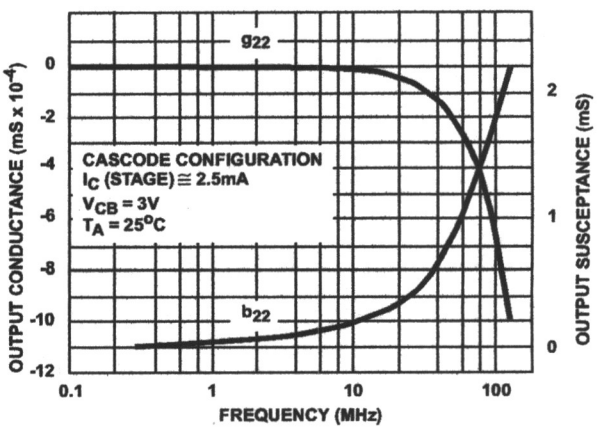


FIGURE 21. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

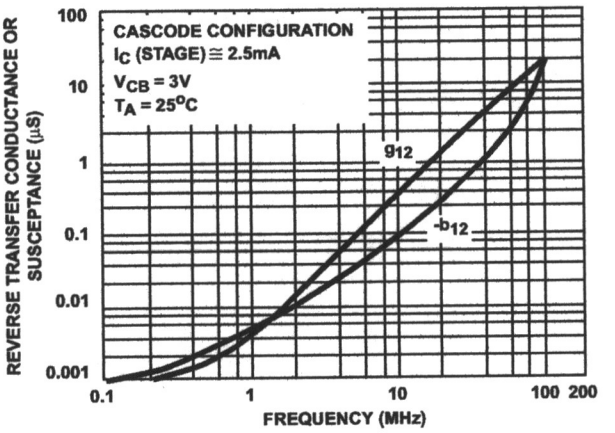


FIGURE 22. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY

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TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

General Purpose NPN Transistor Array

The CA3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

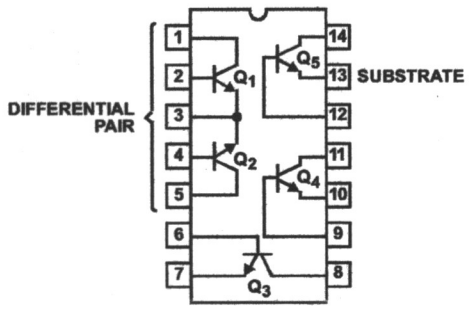
The transistors of the CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3046	-55 to 125	14 Ld PDIP	E14.3
CA3046M (3046)	-55 to 125	14 Ld SOIC	M14.15
CA3046M96 (3046)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Pinout

CA3046 (PDIP, SOIC)
TOP VIEW



Features

- Two Matched Transistors
  - V_{BE} Match . . . . . ±5mV
  - I_{IO} Match. . . . . .2μA (Max)
- Low Noise Figure . . . . . 3.2dB (Typ) at 1kHz
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120MHz
- Wide Operating Current Range
- Full Military Temperature Range

Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

Absolute Maximum Ratings

Collector-to-Emitter Voltage (V_{CEO}) 15V
Collector-to-Base Voltage (V_{CBO}) 20V
Collector-to-Substrate Voltage (V_{CIO}, Note 1) 20V
Emitter-to-Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 50mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	180	N/A
SOIC Package	220	N/A

Maximum Power Dissipation (Any One Transistor) 300mW
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$T_A = 25°C$, characteristics apply for each transistor in CA3046 as specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$		5	7	-	V
Collector Cutoff Current (Figure 1)	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$		-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$		-	See Fig. 2	0.5	µA
Forward Current Transfer Ratio (Static Beta) (Note 3) (Figure 3)	h_{FE}	$V_{CE} = 3V$	$I_C = 10mA$	-	100	-	-
			$I_C = 1mA$	40	100	-	-
			$I_C = 10\mu A$	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO1} - I_{IO2} \rvert$ (Note 3) (Figure 4)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.3	2	µA
Base-to-Emitter Voltage (Note 3) (Figure 5)	V_{BE}	$V_{CE} = 3V$	$I_E = 1mA$	-	0.715	-	V
			$I_E = 10mA$	-	0.800	-	V
Magnitude of Input Offet Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2} \rvert$ (Note 3) (Figures 5, 7)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4} \rvert$, $\lvert V_{BE4} - V_{BE5} \rvert$, $\lvert V_{BE5} - V_{BE3} \rvert$ (Note 3) (Figures 5, 7)		$V_{CE} = 3V$, $I_C = 1mA$		-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 3V$, $I_C = 1mA$		-	-1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1mA$, $I_C = 10mA$		-	0.23	-	V
Temperature Coefficient: Magnitude of Input Offset Voltage (Figure 7)	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	$V_{CE} = 3V$, $I_C = 1mA$		-	1.1	-	µV/°C
DYNAMIC CHARACTERISTICS							
Low Frequency Noise Figure (Figure 9)	NF	$f = 1kHz$, $V_{CE} = 3V$, $I_C = 100\mu A$, Source Resistance = 1kΩ		-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics							
Forward Current Transfer Ratio (Figure 11)	h_{FE}	$f = 1kHz$, $V_{CE} = 3V$, $I_C = 1mA$		-	110	-	-
Short Circuit Input Impedance (Figure 11)	h_{IE}	$f = 1kHz$, $V_{CE} = 3V$, $I_C = 1mA$		-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 11)	h_{OE}	$f = 1kHz$, $V_{CE} = 3V$, $I_C = 1mA$		-	15.6	-	µS

Electrical Specifications $T_A = 25^oC$, characteristics apply for each transistor in CA3046 as specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Circuit Reverse Voltage Transfer Ratio (Figure 11)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	1.8×10^{-4}	-	-
Admittance Characteristics						
Forward Transfer Admittance (Figure 12)	Y_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	31 - j1.5	-	-
Input Admittance (Figure 13)	Y_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	0.3 + j0.04	-	-
Output Admittance (Figure 14)	Y_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	0.001 + j0.03	-	-
Reverse Transfer Admittance (Figure 15)	Y_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA	-	See Fig. 14	-	-
Gain Bandwidth Product (Figure 16)	f_T	V_{CE} = 3V, I_C = 3mA	300	550	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3V, I_C = 0	-	2.8	-	pF

NOTE:

3. Actual forcing current is via the emitter for this test.

Typical Performance Curves

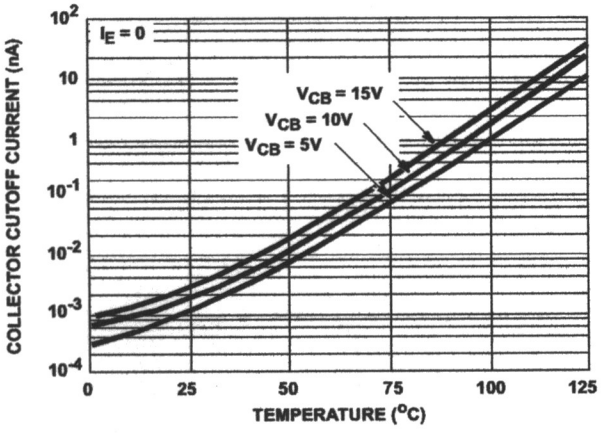


FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

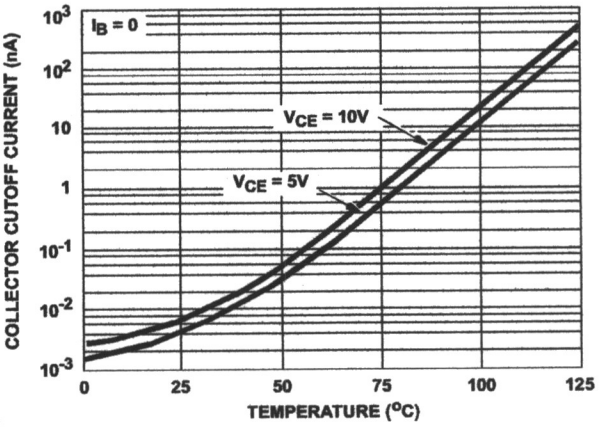


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

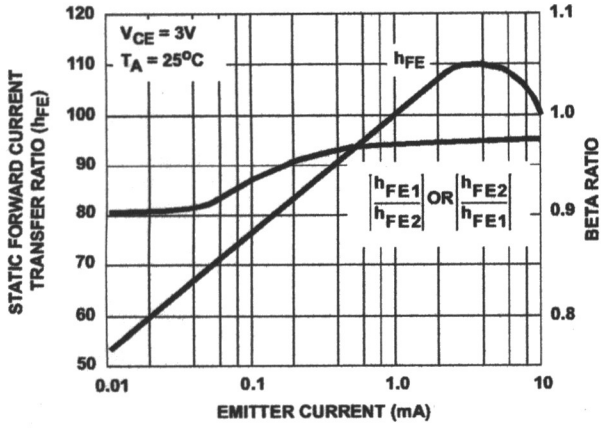


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR Q_1 AND Q_2 vs EMITTER CURRENT

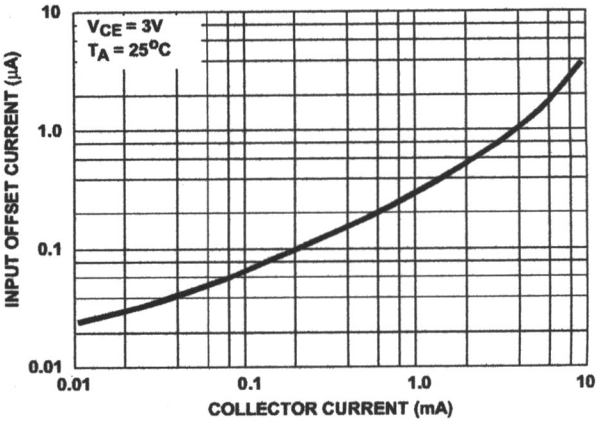


FIGURE 4. TYPICAL INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q_1Q_2 vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

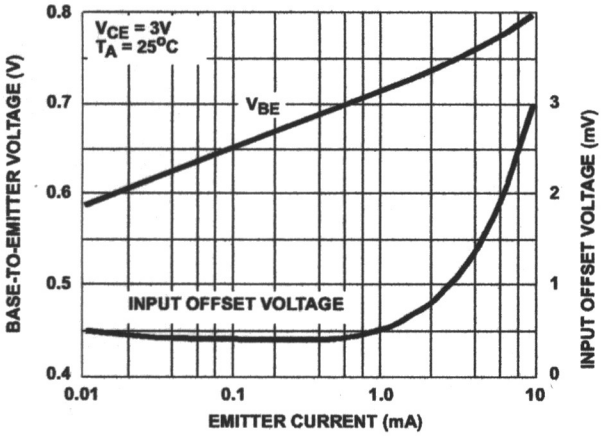


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTICS AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs EMITTER CURRENT

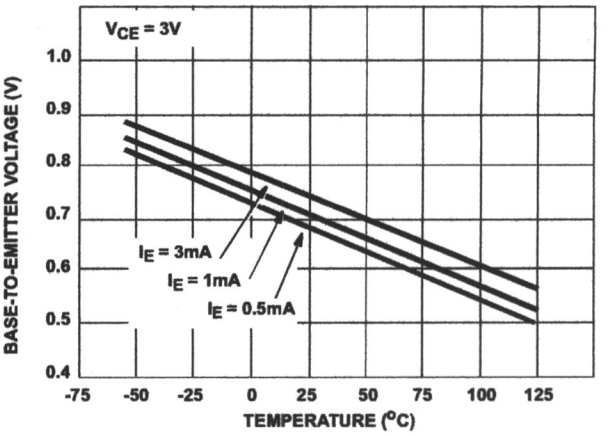


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC vs TEMPERATURE FOR EACH TRANSISTOR

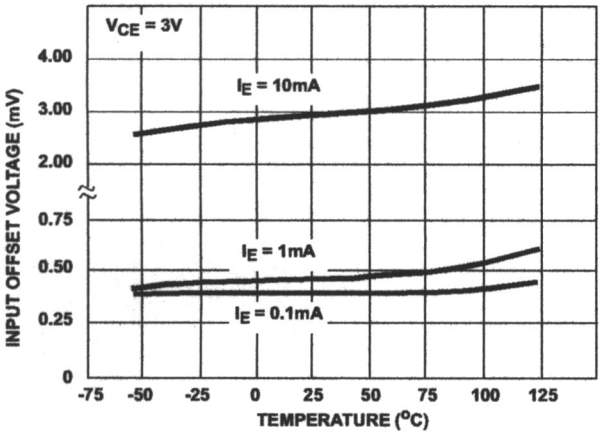


FIGURE 7. TYPICAL INPUT OFFSET VOLTAGE CHARACTERISTICS FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs TEMPERATURE

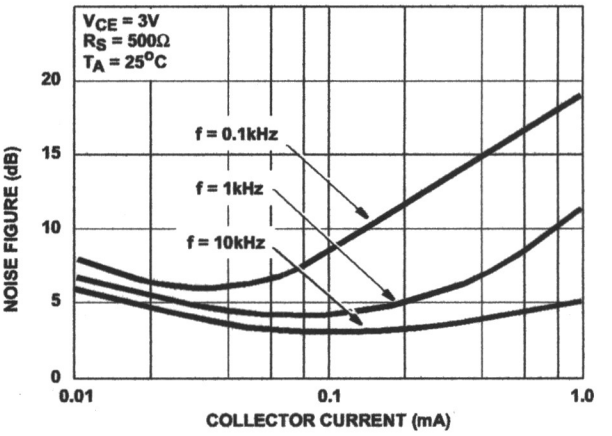


FIGURE 8. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

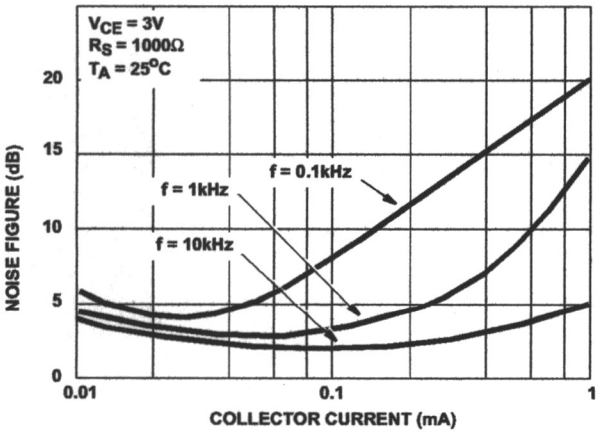


FIGURE 9. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

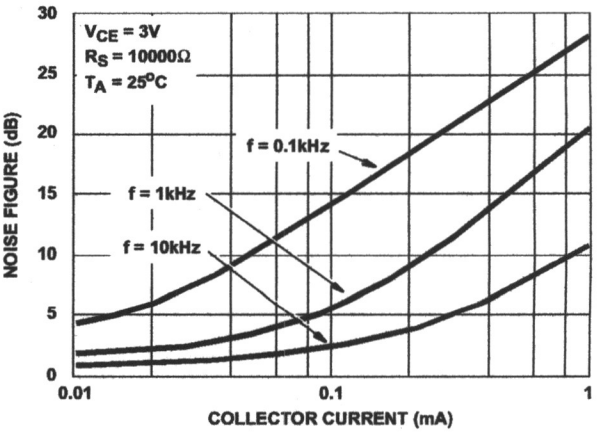


FIGURE 10. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

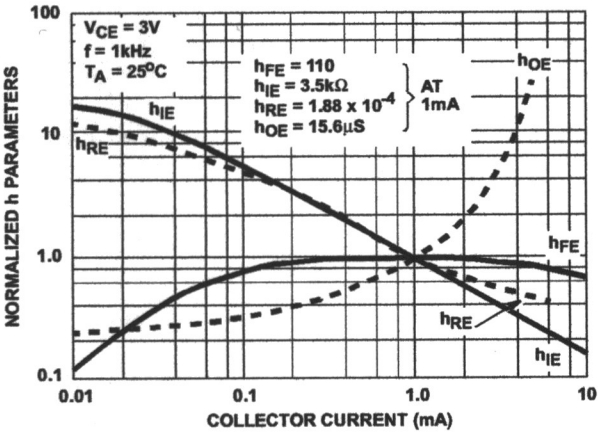


FIGURE 11. TYPICAL NORMALIZED FORWARD CURRENT TRANSFER RATIO, SHORT CIRCUIT INPUT IMPEDANCE, OPEN CIRCUIT OUTPUT IMPEDANCE, AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO vs COLLECTOR CURRENT

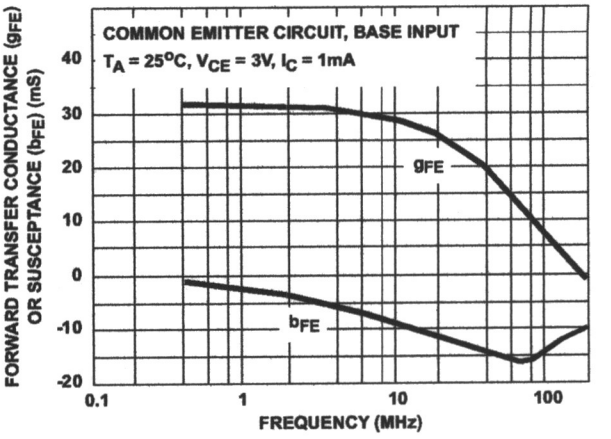


FIGURE 12. TYPICAL FORWARD TRANSFER ADMITTANCE vs FREQUENCY

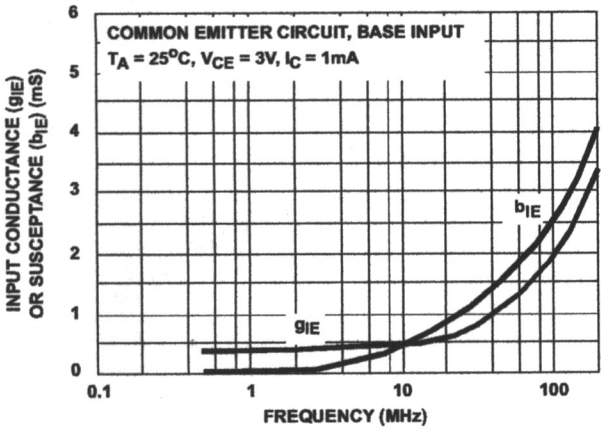


FIGURE 13. TYPICAL INPUT ADMITTANCE vs FREQUENCY

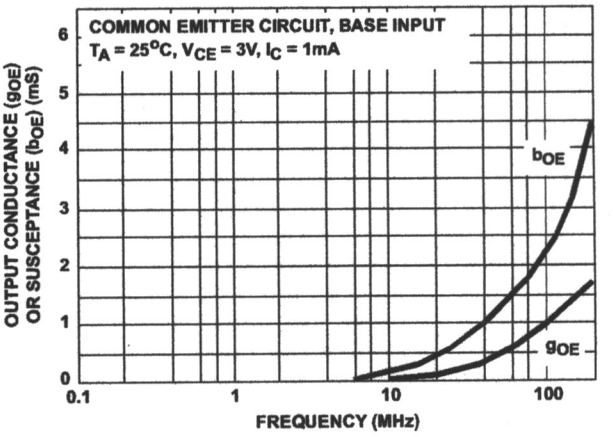


FIGURE 14. TYPICAL OUTPUT ADMITTANCE vs FREQUENCY

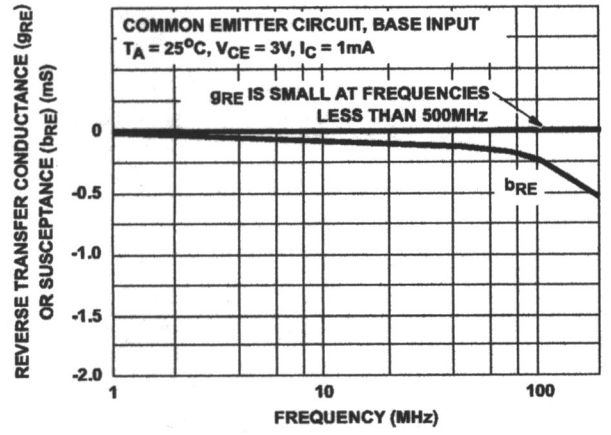


FIGURE 15. TYPICAL REVERSE TRANSFER ADMITTANCE vs FREQUENCY

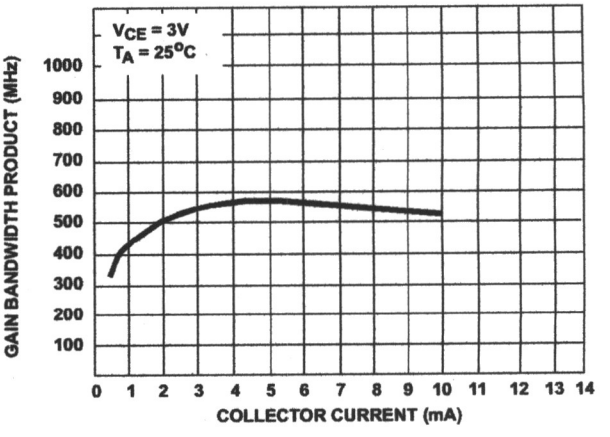


FIGURE 16. TYPICAL GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

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Mercure Center
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1130 Brussels, Belgium
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FAX: (32) 2.724.22.05

ASIA
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Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX: 886-2-2515-8369

CONRAC

7211 C19 4,559
-1590
8wk

Features

- Precision In-line CRT Technology
- Wideband Video Amplifier
- Selectable Horizontal Scan Frequency
- High Density Shadow Mask CRT's
- Pre-set Calibration Controls
- Dynamic Focus
- Modular Electronics Package
- Selectable CRT Resolution

Applications

The models 7111 and 7211 form a family of RGB (Red, Green, Blue) color image displays intended for computer data/graphic applications. These units are specially designed to offer users favorable price vs. performance selection of products best suited for a particular application. Conrac data-graphic monitors are widely used in industrial control, power, water and traffic management, CAD/CAM and various other color data display applications.

Descriptive Information

The models 7111 and 7211 are raster scan RGB (Red, Green, Blue) color image display monitors which, aside from the picture tubes, are identical. The models 7111 and 7211 feature (Precision In-line Gun), picture tube technology, which virtually eliminates routine convergence adjustments. The 7211 series utilizes a high-resolution dot-matrix shadow mask CRT featuring .31 mm (0.11 in.) pitch. Both models 7111 and 7211 are available in 13″ and 19″ diagonal screen sizes.

The advanced design of the electronic circuitry in these displays is such that the picture tube itself is the limiting factor. The three RGB color inputs will accept either standard EIA RS170 or high-resolution EIA RS343 composite video format. A separate sync input allows the units to accept non-composite video at the RGB inputs and composite sync from a separate line. A keyed back-porch clamp maintains true black level when operating composite or non-composite video input. Operator conveniences include the addition of preset controls for brightness and contrast calibration in all model configurations.

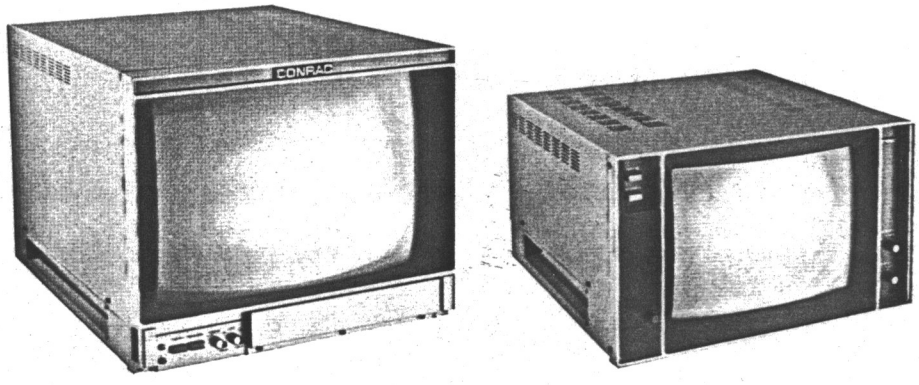
All units comply with the U.S. Department of Health and Human Services X-Radiation Safety Rules, 21 CFR, Subchapter J, applicable at time of manufacture and are U.L. listed.

The 7111, 7211 series is manufactured in Covina, California, USA by the Conrac Division of Conrac Corporation.

7111/7211

Raster Scan Color Displays

For Alphanumeric, Graphic Display and Medical Imaging Applications



Specifications

Operator Controls

Contrast w/preset Calibration
Brightness w/preset Calibration
Power On/Off
Degauss Momentary Push Button

Secondary Controls

Red, Green, Blue Gun on/off Switches
Red, Green, Blue Low Light Calibration
Video Input Test Channel Select Switch

Channel A

Three loop-through BNC type connectors are provided with switchable high Z or 75 Ohm termination.

Channel B

A loop-through monochrome input is provided.

External composite sync is provided with loop-through capability.
Internal or external sync is selectable by a jumper plug located on the video module.

Long Persistence Phosphor
Anti-glare Screens
Differential Video Input
Rack Slide, Cabinet or Naked Configurations
External Horizontal & Vertical Drive

Signal Inputs

Composite for each of the three RGB Inputs IV P-P nominal (.35V - 2.0V) acceptable. Sync negative.
Non-composite for each of the three RGB inputs .7V nominal (.25V - 1.4V) acceptable. Black negative.

External Sync

4V P-P nominal (1V to 8V) acceptable. Negative.
All inputs are RS170 compatible for 15.75KHz operation or RS343 for 36.75KHz operation.
Return loss: greater than 40 db

Sync and Deflection Characteristics

Scan Rates: 15.750 KHz through 36.75 KHz interlaced or noninterlaced. Scanning rates are determined by jumper plug selection on scan module.
Horizontal retrace: 5 usec nominal.
Vertical retrace: 550 usec nominal.
Interlace performance: better than 90%
Raster size regulation: less than 1% change from 0 to 100% APL at 20 FL.
Scan failure protection: ultor voltage is switched off in the event of scan failure.

Video Characteristics

Video Bandwidth: −3 db 40 MHz
Pulse Performance: TR = 10 nsec, TF = 13 nsec
Line Distortion: less than 1%
Field Distortion: less than 1%
Black level stability: black level shift less than 1% change of peak luminance from 10% to 90% APL.

Display Performance

Picture tube standard resolution black matrix CRT
Pitch 13″ — .63 mm (0.24 in)
19″ — .79 mm (0.31 in)
High resolution black matrix CRT
Pitch 13″ & 19″ — .31 mm (0.118 in)
Geometric distortion ± 2% of raster height.

Actual display area

19″ CRT	13″ CRT
1176.1 Sq cm	571.3 Sq cm
(180.0 Sq in)	(88.5 Sq in)
29.7 cm high	20.7 cm high
(11.6 in)	(7.92 in)

Actual display area (continued)

39.6 cm wide (15.5 in)	27.6 cm wide (10.8 in)

Aspect Ratio adjusted at factory 4 to 3 underscan. Other aspect ratios available on special order.

Maximum allowable convergence error over the entire display area.

.7 mm	13″ CRT
1.0 mm	19″ CRT

Brightness

Maximum usable brightness

13″ 80 FL	19″ 50 FL

Calibration

13″ 30 FL	19″ 30 FL

Calibration is achieved with brightness at visual CRT cutoff and contrast adjusted with flat field signal.

Typical Display Resolution at 1225 line scan

19″ Standard Resolution:	503 horizontal x 576 vertical
19″ High Resolution:	1080 horizontal x 809 vertical
13″ Standard Resolution:	427 horizontal x 517 vertical
13″ High Resolution:	921 horizontal x 739 vertical

Power Requirements
Power Selection

100 VAC ± 10%
170 VAC ± 10%
200 VAC ± 10%
220 VAC ± 10%
234 VAC ± 10%

Frequency

50-60 Hz ± 10%

Power Consumption

275 Watts nominal

Operating Environment

Temperature:	0° to 50°C
Humidity:	10% to 90%, non-condensing
Altitude:	Normal operation to 10,000 Feet

Safety

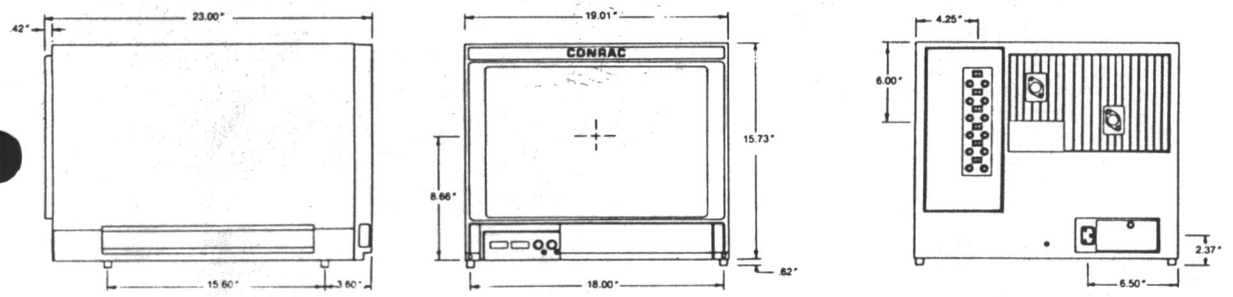
Per applicable DHHS, UL, CSA as date of manufacture

Physical characteristics

13″ Weight 62 pounds
Rack mount 19″ wide, 10.47″ high, 18.3″ deep
Cabinet 17.6″ wide, 10.47″ high, 18.3″ deep
19″ Weight 93 pounds
Rack mount 19″ wide, 15.70″ high, 22.3″ deep
Cabinet 19″ wide, 15.70″ high, 22.3″ deep

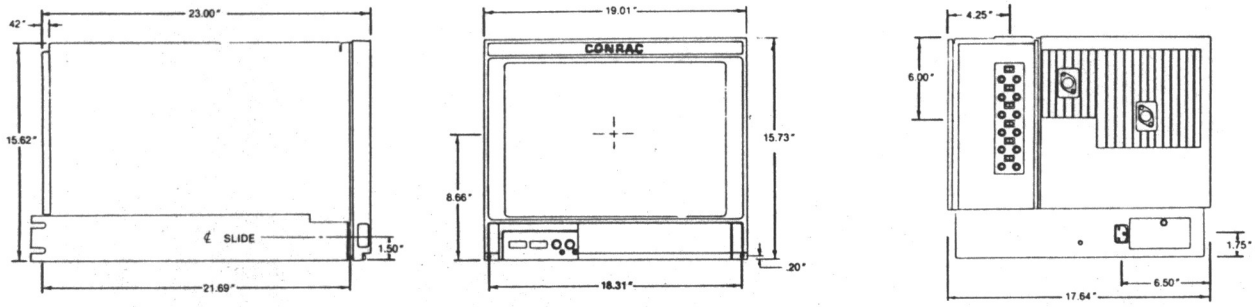
Outline Dimensions

7111/7211C19

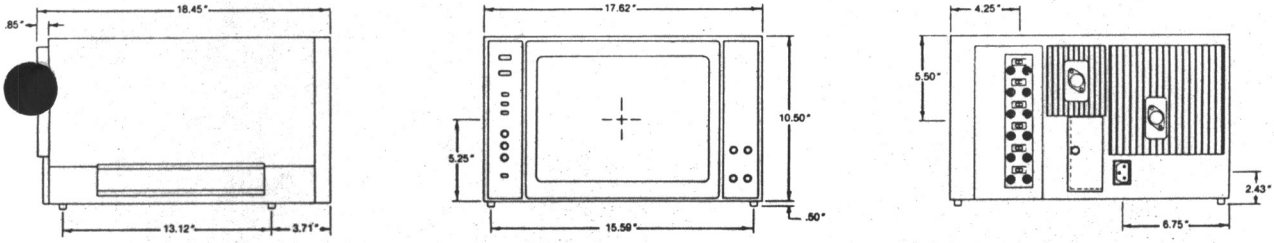


Outline Dimensions (Continued)

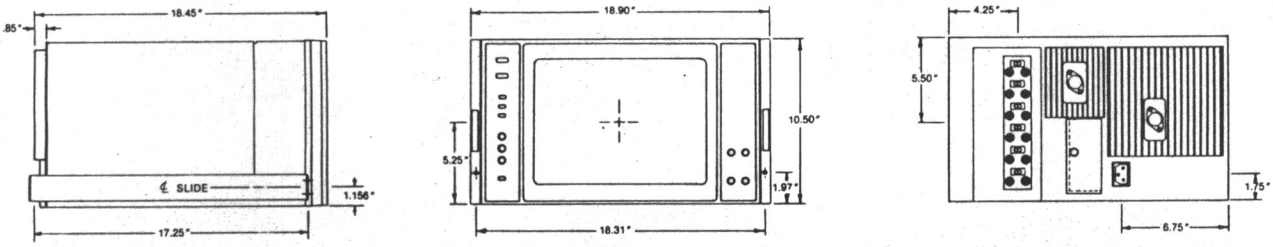
7111/7211RS19



7111/7211C13



7111/7211RS13



CONRAC

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Printed in U.S.A.

Matthey

NEW EDITION

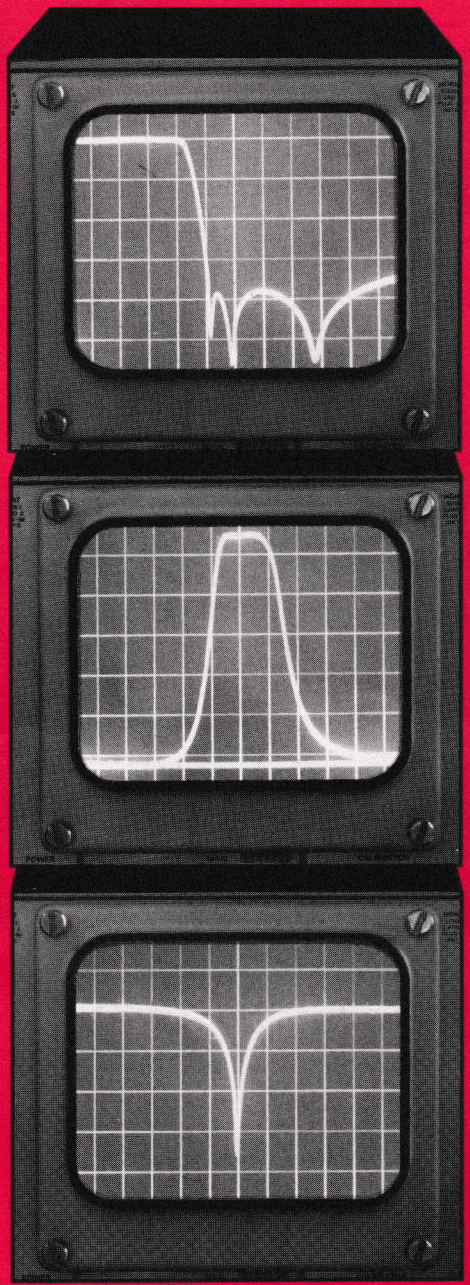
VIDEO FILTERS

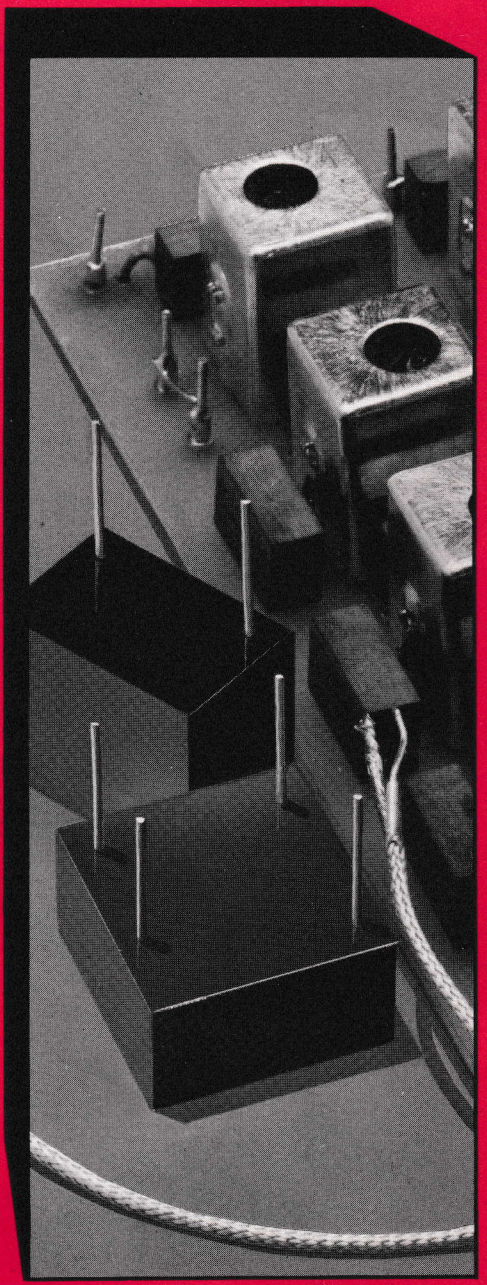
Filtres Vidéo
Video-Filter

Filtros Video
Видеофильтры

視頻濾波器

ヴィデオ・フィルター





2035 A
October 1977

In colour Television Broadcasting or CCTV it is often desirable to use a passive filter to deal with a special problem. Engineers often decide to build such a filter because it is difficult to find a good quality low cost unit available for quick delivery.

This booklet gives the details of the full range of Matthey Filters available. We acknowledge the initial help given by the British Broadcasting Corporation from which this large range has been developed.

For studio engineers the filters have 75Ω impedance and BNC connectors for easy connection in the Video signal path. For equipment manufacturers both 75Ω and 510Ω units are provided in small size ready for inserting into their own equipment racks or printed circuit boards.

Matthey Filter engineers are able to design special units not included in this booklet.

- Pour une introduction en votre langue voir la page 12 .
- Einführung in Ihrer Sprache siehe S.12
- Véase página 12 para una introducción en su idioma.
- Введение на Вашем языке на странице 12 .
- 第十二页是用贵国文字写的介绍
- '日本語による御案内は12ページです'

CONTENTS


Matthey
LOW PASS VIDE
with phase equ
75Ω
Matthey
FRM 443 CB
REJECTION FILTER
(colour sub carrier)
75Ω
4·43 MHz
MANUFACTURED BY Matthey Printed Products Limited BURSLEM U.K.
Matthey
FPM 443 AB
PASS FILTER
(colour sub carrier)
4·43 MHz
75Ω
MADE BY Matthey Printed Products Limited BURSLEM U.K.
Matthey
FRM 358 AB
REJECTION FILTER
(colour sub carrier)
3·58 MHz
75Ω
MADE BY Matthey Printed Products Limited BURSLEM U.K.
Matthey FIM/A
MADE IN UK 7548
IN 7520 OUT
Matthey
M200/47015
Pt 1
MADE IN UK
Matthey
FPM 443 AE
MADE IN UK
7548
Matthey
FQM/A
MADE IN UK
7548
Matthey FRM358BE
MADE IN UK 7548
Matthey
FRM358 AE
MADE IN UK
7548

VIDEO FILTERS

Application Data

Matthey filters are used by many organisations throughout the World. This catalogue outlines the various filters of special interest to television station engineers and studio equipment manufacturers. The four types outlined are:

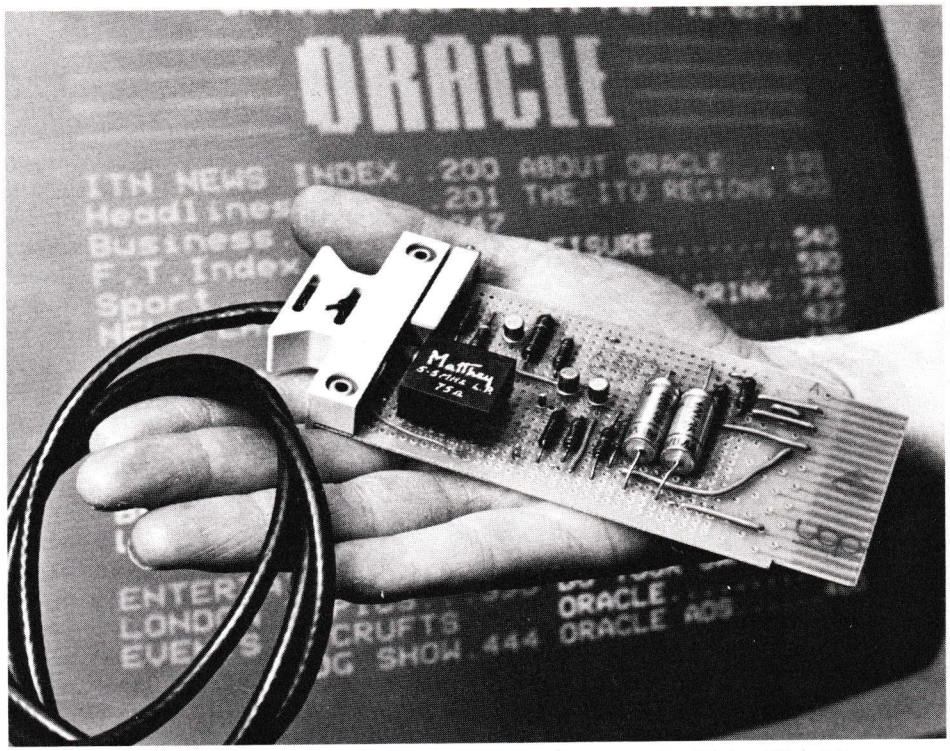
1. A series of phase compensated low pass filters intended for band limitation of systems. Listed as the FLM range, twenty-seven versions are currently available to give a wide choice of cut-off frequency between 0.2 MHz and 10 MHz.

2. A series of low pass Gaussian Filters. These take the form of small encapsulated modules suitable for installation in equipments. They are used for such applications as: The production of limited bandwidth pulses e.g. television synchronization pulses; removing overshoot and ringing from pulses; and producing pulses approximating to a Gaussian shape.

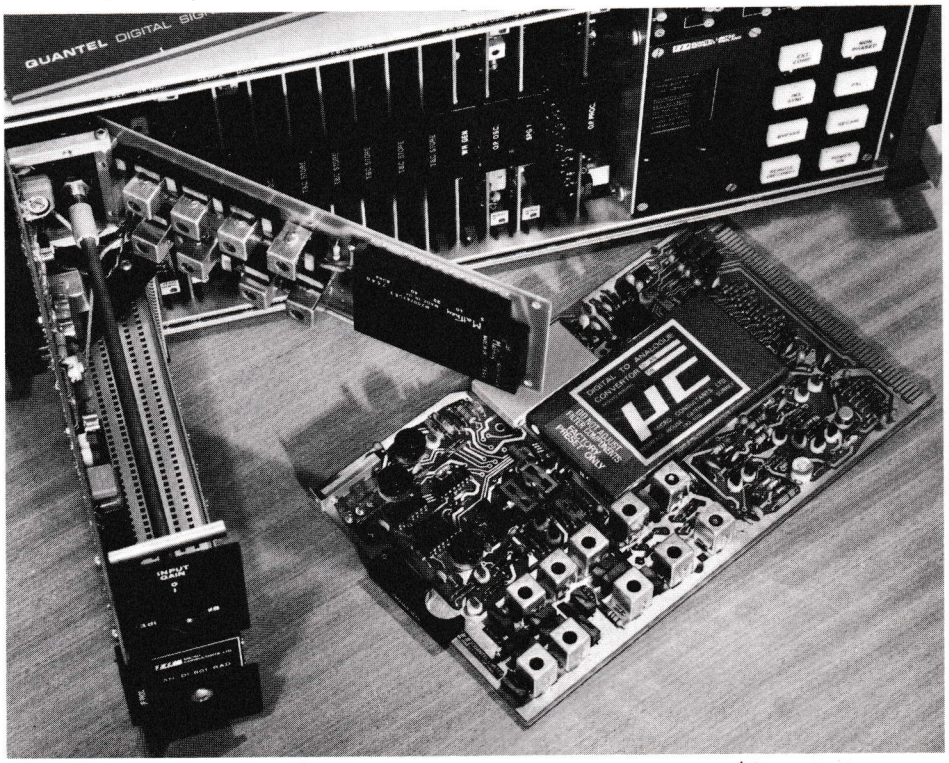
3. Colour Sub-Carrier Rejection and Pass Filters. The rejection filters suppress the colour information in the Video signal to allow isolation of the luminance information. The Pass filters suppress the luminance to allow isolation of the colour information. A number of filters for both the PAL and NTSC systems are available in boxed, encapsulated and P.C.B. form.

4. CFLM, HFM and SFLM Low Pass Filters are designed for improved and special performances in both analogue TV and digital TV processing equipment. Special attention has been paid to the requirements of A/D and D/A converters.

If you have a filter requirement outside the types covered here please contact us. We provide a computer aided design and manufacturing service for LC Filters and will be pleased to examine your problem.



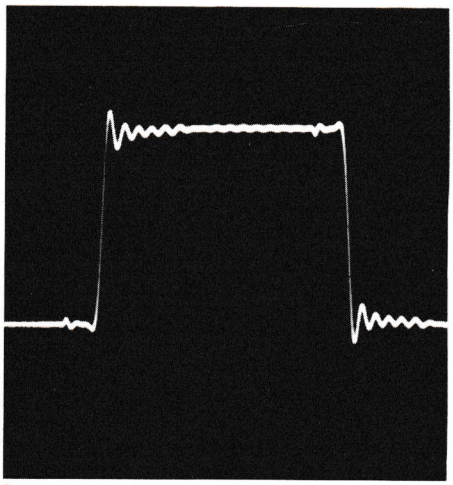
1 Matthey Gaussian Filter used in ORACLE System — Courtesy of London Weekend Television



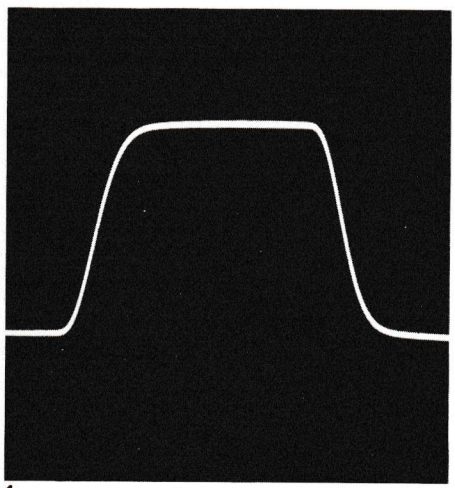
2 Matthey FLM Range Filters used in Digital Signal Processor — Courtesy of Quantel Ltd

VIDEO FILTERS

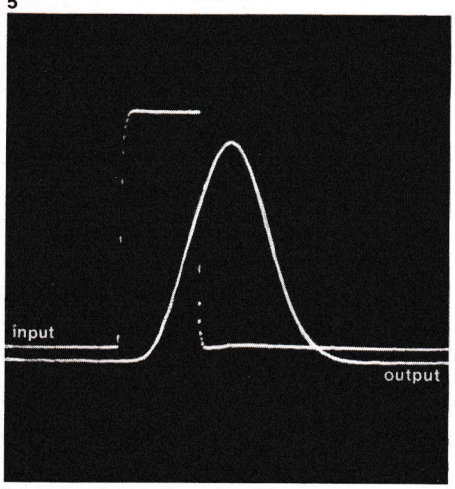
Gaussian Filters



3 Pulse In



4
5 Pulse Out



An approximate Gaussian Waveshape obtained by passing a pulse through a Matthey Gaussian Filter.

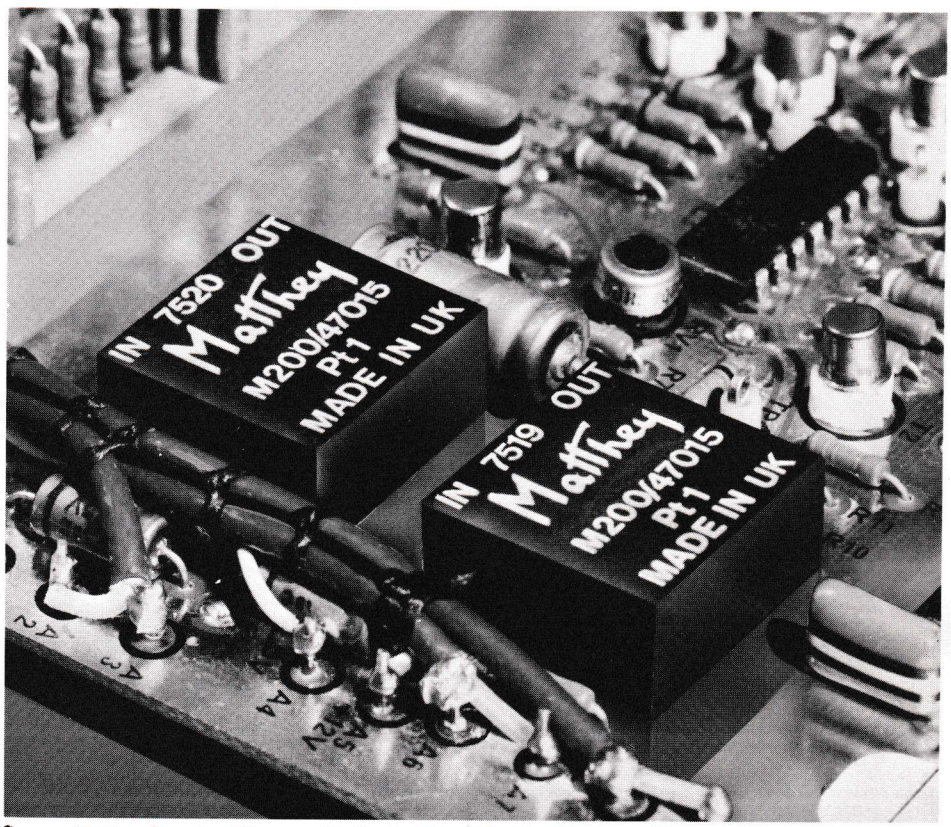
These low pass filters derive their name from the fact that the amplitude/frequency response is an approximation to a Gaussian distribution.

Matthey Gaussian Filters are used for pulse shaping and bandwidth limitation. They are also used to remove unwanted distortions such as noise, ringing, overshoot and preshoot. For example, high frequency components in video line sync. pulses can cause spikes or severe ringing. Gaussian Filters 47015 parts 1, 2 and 3, will remove these components and meet the CCIR recommendation for the sync. pulse leading edge of 250 ± 50 ns. (See photographs 3 and 4).

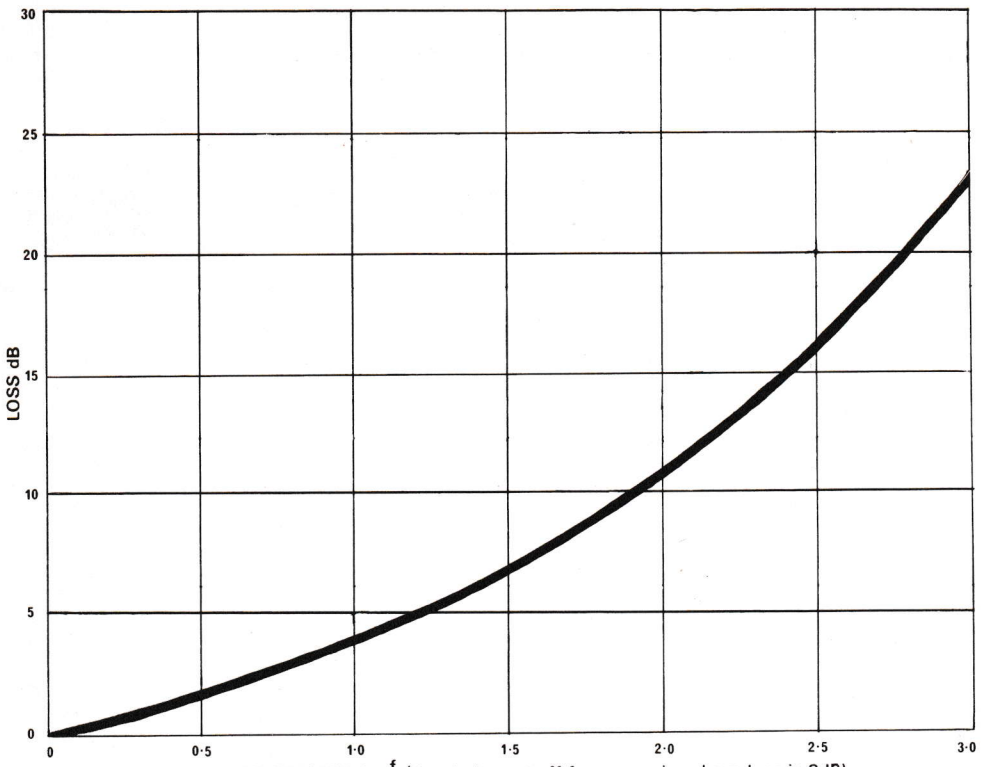
If a rectangular pulse with a width approximately equal to that of the nominal rise time of the filter is applied to the input of the network, an approximation to a Gaussian waveshape will be obtained at the output. (See photograph 5).

Given the width of the input pulse, Matthey can advise on the relationships between the amplitude of the output pulse and the bandwidth of the filter.

An application which is particularly relevant concerns shaping the bit-stream emerging from the A - D converter in systems for transmitting data in the field blanking period of Television signals. A similar application is found in the sound-in-syncs. system, developed by the B.B.C.



6 Matthey Gaussian Filters used in Caption Edger Module—Courtesy of Prowest Electronics Ltd



Loss v Frequency Curve for Matthey Gaussian Filter

The twenty seven versions currently available are shown in the table below. Requests for versions other than those shown in the table will be welcomed.

The parameters which should be specified are:

(i) the impedance

(ii) the 3dB frequency **or** rise time.

Technical Data — Gaussian Filters

Nominal f3dB	Module Number	Source and Load Impedance	Nominal Frequency at which loss >17dB w.r.t. 100 KHz	Nominal Delay Time	Nominal Rise Time	Encaps. Size*
MHz		*Ω*	*MHz*	*ns*	*ns*	
0.17	47015/18	510	0.45	1988	2016	2
0.30	47015/4	510	0.80	1126	1147	2
0.33	47015/19	510	0.87	1024	1038	2
1.00	47015/27	75	2.60	340	357	2
1.00	47015/22▽	510	2.60	338	343	2
1.14	47015/12▽	50	3.00	296	300	2
1.14	47015/28	75	3.00	296	300	2
1.25	47015/2	75	3.30	270	275	2
1.50	47015/3	75	4.00	225	229	2
1.50	47015/1	510	4.00	225	229	2
1.72	47015/5	75	4.50	196	200	2
1.72	47015/6	510	4.50	196	200	2
2.00	47015/16▽	50	5.20	169	171	2
2.00	47015/26	75	5.20	169	171	2
2.00	47015/21▽	510	5.20	169	171	2
2.39	47015/20▽	510	6.30	142	144	2
2.50	47015/29	75	6.60	148	137	2
3.00	47015/7	75	8.00	113	115	2
3.44	47015/8	75	9.00	98	100	2
3.44	47015/9	510	9.00	98	100	2
4.00	47015/10	75	10.50	84	86	2
4.00	47015/25	510	10.50	84	86	2
4.89	47015/24▽	510	12.80	68	70	2
5.00	47015/11	75	13.20	67	69	2
5.53	47015/30	75	14.65	67	62	2
12.00	47015/15	75	32.00	29	28	2
15.00	47015/23	75	39.00		23	2

▽ Both earth pins must be connected

* For dimensions see page 11

VIDEO FILTERS

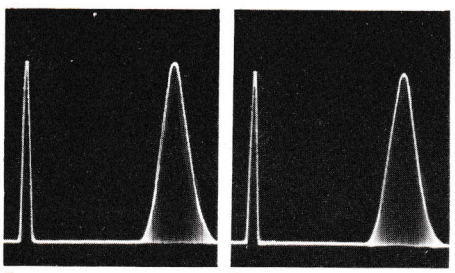
Low Pass Filters

The filters in this series are suitable for band limitation in various systems.

Based on a B.B.C. design, the 7th order elliptic function low pass filter has a relatively sharp cut-off and a flat pass band. Three constant resistance sections provide phase compensation in the pass band. This together with a design impedance of 75Ω makes them useful for many applications especially in PAL, NTSC and SECAM television systems. The range was originally developed for such systems, examples of use being: noise suppression; separation of Audio from Video (the fast rate of cut-off is essential here); band limitation when using a V.T.R. of restricted bandwidth to enable a wider range of material to be recorded at a reasonable quantity level.

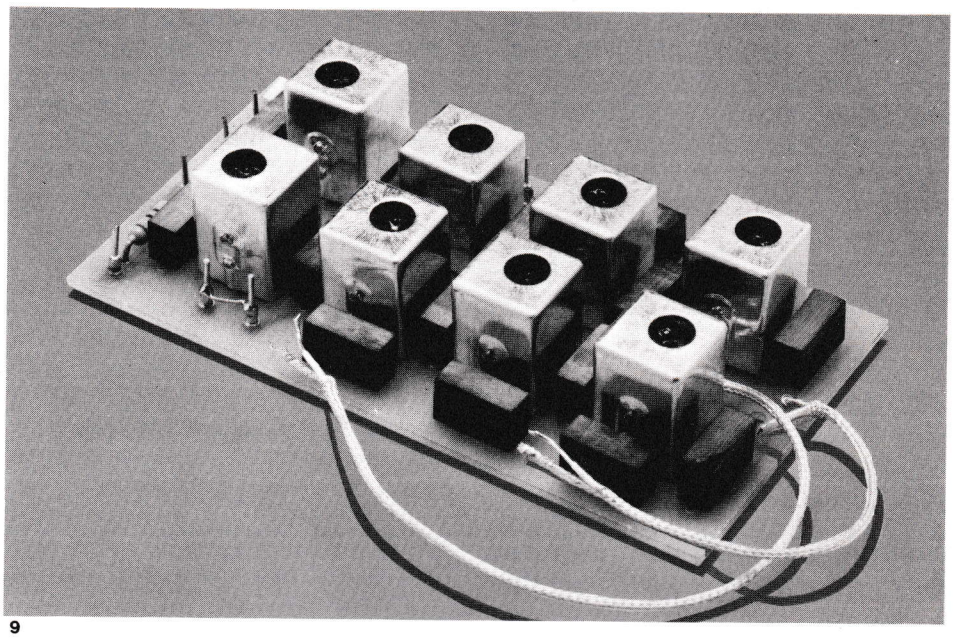
Although the present range allows a wide choice of cut-off frequency, others can be designed if a suitable one is not shown in the table.

The filters can be supplied in a die-cast box fitted with either BNC or MUSA connectors or built onto a P.C.B. fitted with flying leads. The latter type is particularly useful for mounting in equipment.



7 Before FLM 550 B 8 After FLM 550 B

Photographs showing degree of phase equalisation provided in the FLM series of filters



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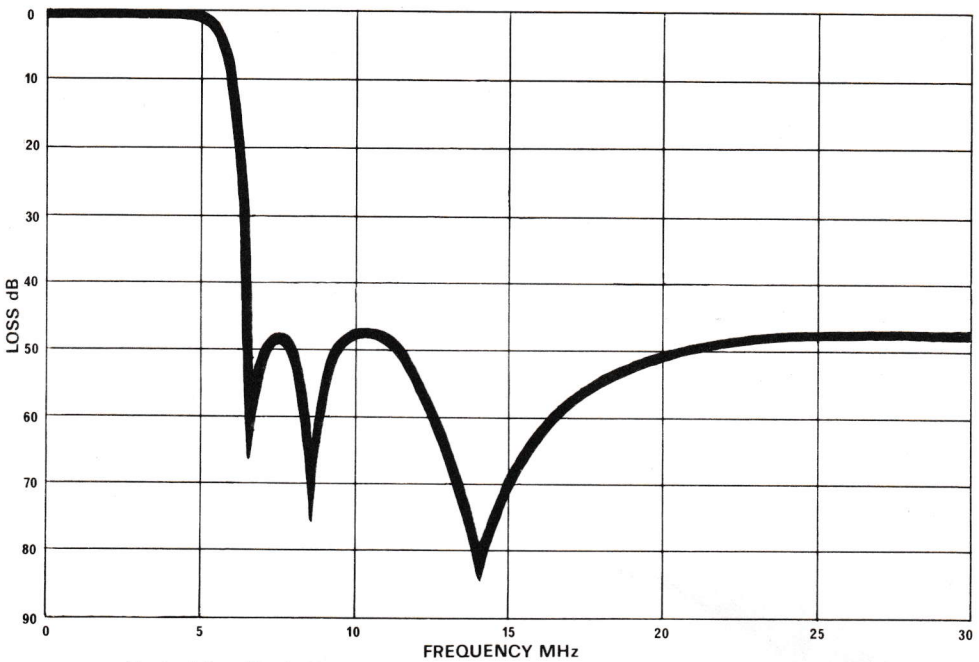
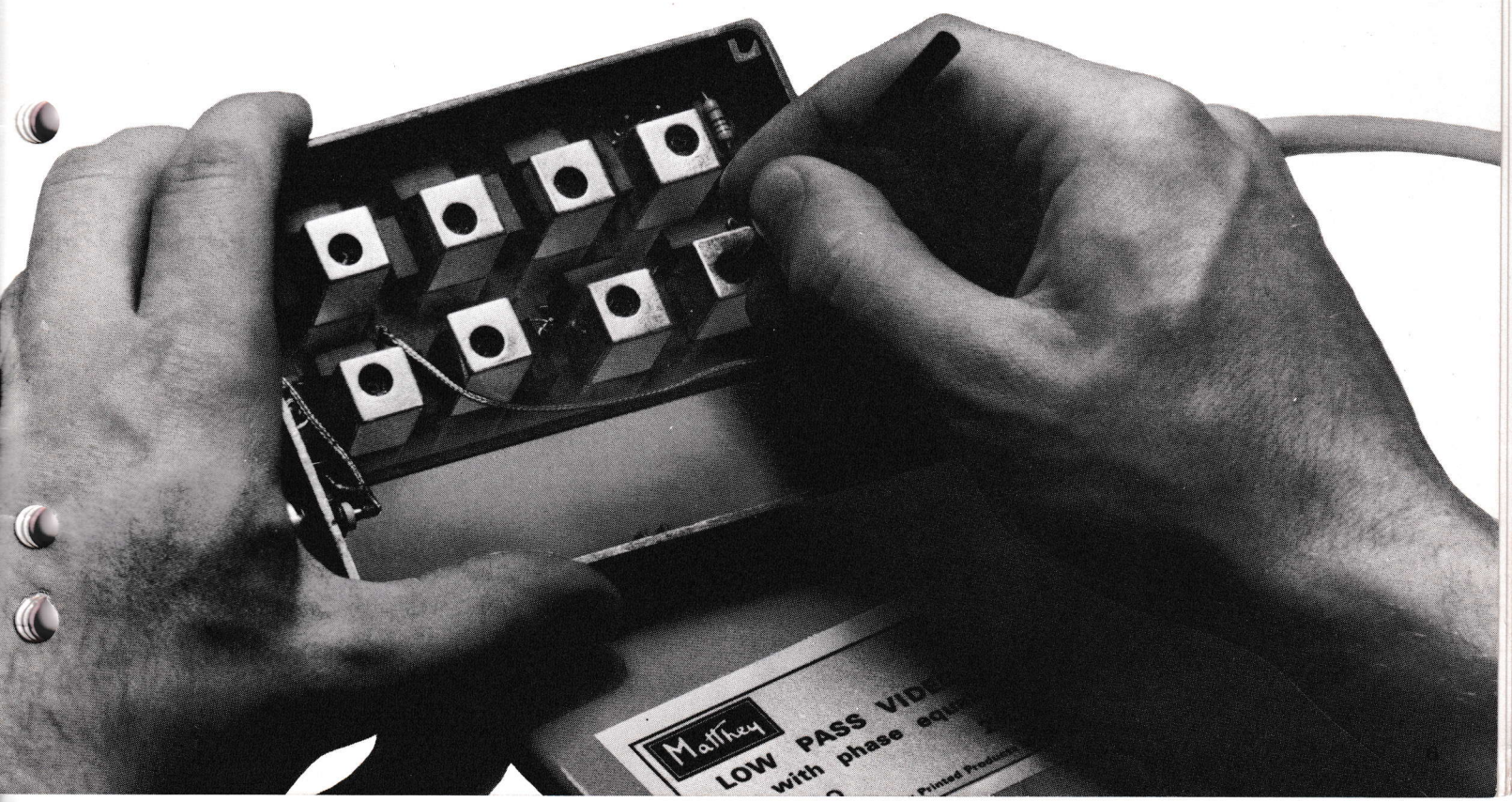


Typical Amplitude Response curve for type FLM 550 P. The other types listed have similar curves scaled to the appropriate frequency range.

Technical Data — Low Pass Filters (FLM Range)

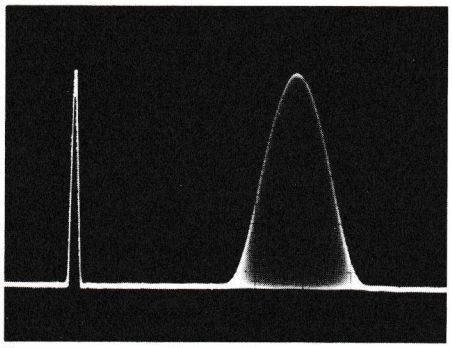
Nominal Frequency *MHz*	Boxed Version	P.C.B. Version	Insertion Loss 3dB w.r.t. 100 KHz at *MHz*	Insertion Loss ≥ 45dB w.r.t. 100 KHz at *MHz*	Delay f = o *ns*	Box Size*	P.C.B. Size*
0.20	FLM 020 B	FLM 020 P	0.20	0.25	14000	B	C
0.50	FLM 050 B	FLM 050 P	0.51	0.63	5520	B	C
1.00	FLM 100 B	FLM 100 P	1.01	1.25	2760	B	C
1.20	FLM 120 B	FLM 120 P	1.22	1.50	2300	B	C
1.25	FLM 125 B	FLM 125 P	1.27	1.57	2208	B	C
1.50	FLM 150 B	FLM 150 P	1.53	1.89	1833	B	C
2.00	FLM 200 B	FLM 200 P	2.03	2.50	1380	B	C
2.50	FLM 250 B	FLM 250 P	2.53	3.13	1104	B	C
2.75	FLM 275 B	FLM 275 P	2.81	3.46	1000	B	C
3.00	FLM 300 B	FLM 300 P	3.04	3.75	920	B	C
3.12	FLM 312 B	FLM 312 P	3.18	3.93	880	B	C
3.50	FLM 350 B	FLM 350 P	3.55	4.38	789	B	C
3.70	FLM 370 B	FLM 370 P	3.81	4.70	736	B	C
4.00	FLM 400 B	FLM 400 P	4.05	5.01	686	B	C
4.25	FLM 425 B	FLM 425 P	4.30	5.31	648	B	C
4.31	FLM 431 B	FLM 431 P	4.40	5.43	638	B	C
4.50	FLM 450 B	FLM 450 P	4.56	5.63	610	B	C
4.80	FLM 480 B	FLM 480 P	4.98	6.06	570	B	C
5.00	FLM 500 B	FLM 500 P	5.10	6.29	550	B	C
5.50	FLM 550 B	FLM 550 P	5.61	6.92	500	B	C
5.59	FLM 559 B	FLM 559 P	5.70	7.03	492	B	C
5.80	FLM 580 B	FLM 580 P	5.92	7.30	474	B	C
6.00	FLM 600 B	FLM 600 P	6.12	7.55	458	B	C
6.50	FLM 650 B	FLM 650 P	6.63	8.18	423	B	C
7.00	FLM 700 B	FLM 700 P	7.14	8.81	393	B	C
7.50	FLM 750 B	FLM 750 P	7.65	9.44	367	B	C
10.00	FLM 1000 B	FLM 1000 P	10.20	12.58	275	B	C

* For dimensions see page 11.

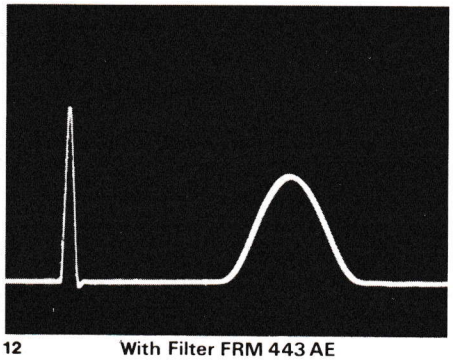


VIDEO FILTERS

Colour Sub-Carrier Filters

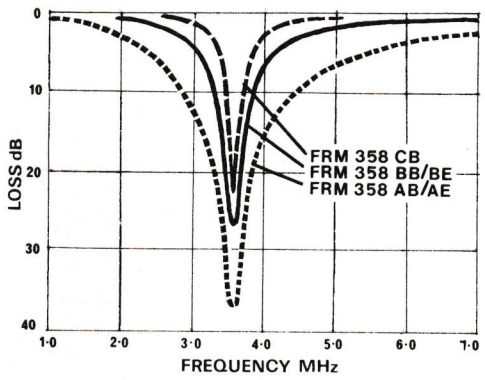


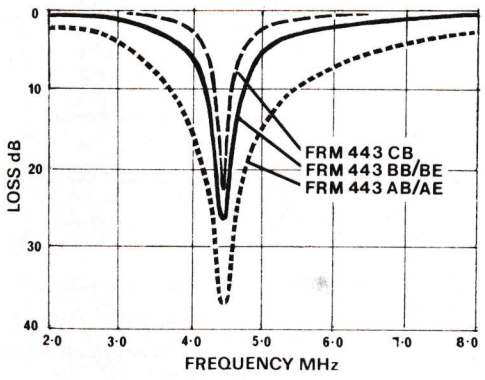
11 Without Filter



12 With Filter FRM 443 AE

Part of Line 17 Pulse & Bar Test Wave Form





Typical Amplitude Responses

Rejection Filters

Matthey sub-carrier rejection filters are band stop filters designed to reduce the level of sub-carrier (3.58 or 4.43 MHz) in NTSC or PAL colour signals. Various organisations require different bandwidths and for this reason three versions for each sub-carrier frequency have been designed. Where necessary the filters employ phase equalisation to minimise distortion of the luminance signal. The design impedance of 75Ω allows direct insertion into the video path.

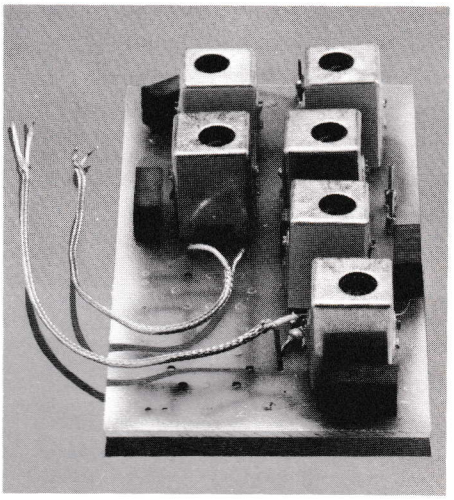
Typical applications of this type of filter are:

(a) Insertion in the video line when monochrome programmes are being broadcast on a colour system. This prevents random flashes of colour from being produced on the receiver screen.

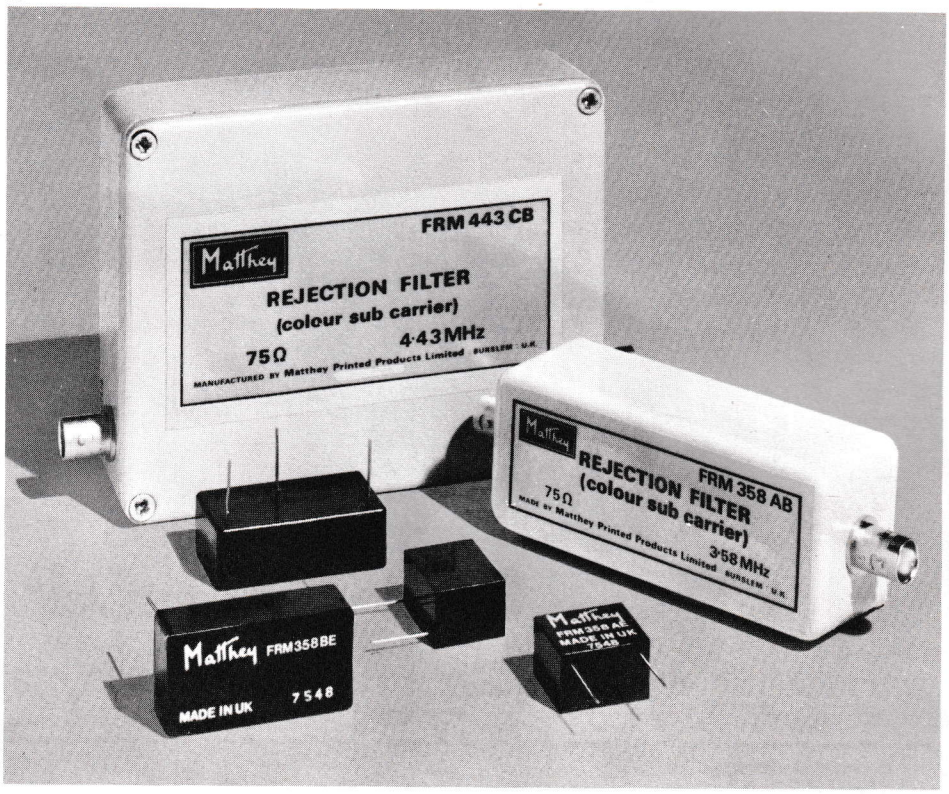
(b) Its use in feeds to monochrome monitors e.g. Camera monitors to prevent interference on the monitor due to colour information. This may be introduced into the feed by cross coupling within the studio system or equipments such as vision mixers.

All six filters are available in metal boxes fitted with BNC Connectors which studio engineers may find most convenient. Equipment manufacturers can select encapsulated modules for two of the types, the third being available in P.C.B. form with flying leads. (See photographs 13 and 14)

14



13

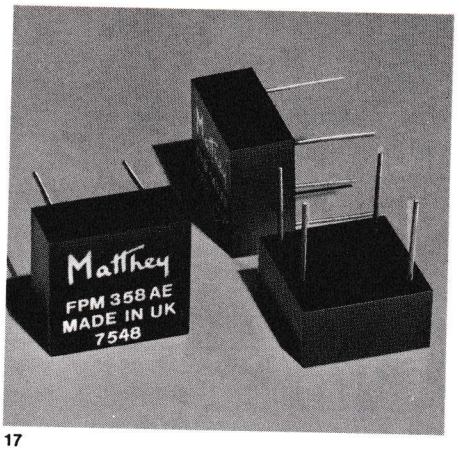


Pass Filters

Matthey sub-carrier pass filters are band pass filters designed to suppress the luminance information in colour TV signals. They are used therefore, in applications where it is necessary to isolate the chrominance information.

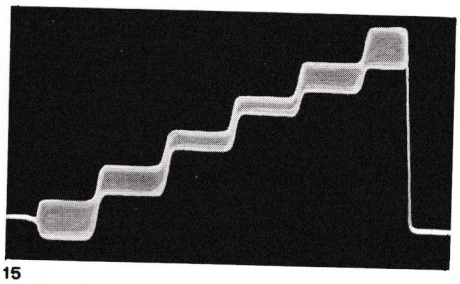
Two filters, one suitable for PAL and one for NTSC are available as either small encapsulated modules or in the form of a die-cast box fitted with BNC Connectors. (See photographs 17 and 18). Their design impedance is 75Ω to facilitate direct use in signal paths.

One use is in the measurement of differential gain. Photo 15 shows a PAL chrominance modulated staircase. Photo 16 shows the same signal after filter FPM/443/AE. The differential gain distortion can now readily be seen and measured.

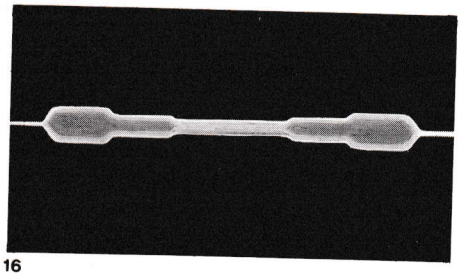


17

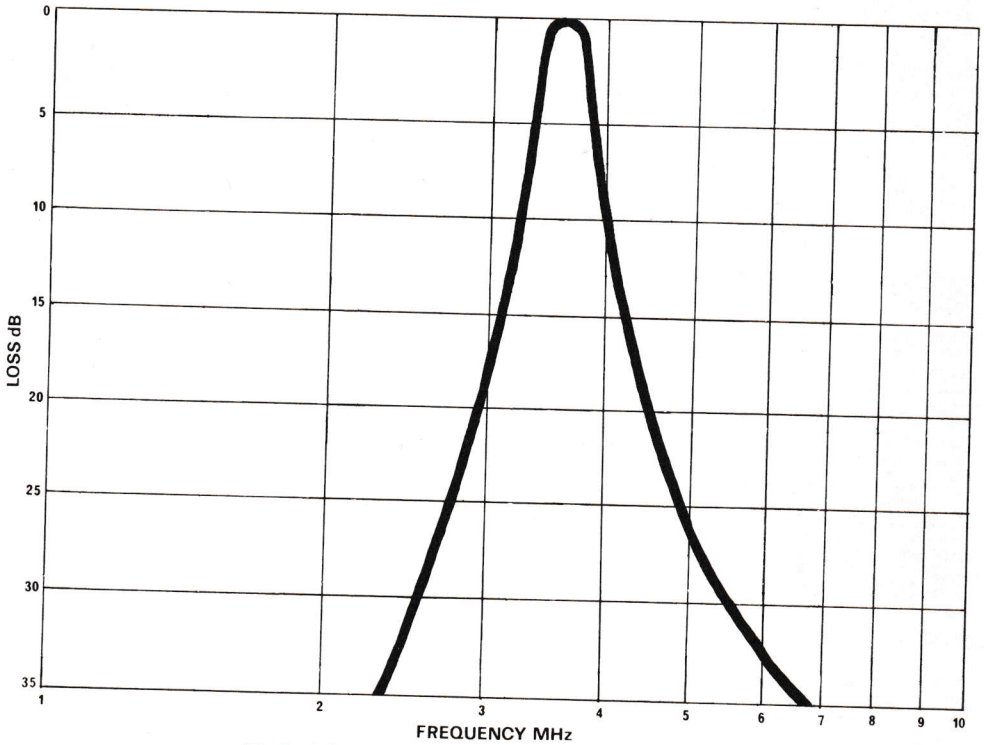
18



15



16



Typical Amplitude Response of type FPM 358 AE

Technical Data — Rejection Filters

TV System	Frequencies at which loss is 3dB w.r.t. 100 KHz *MHz*	Box Version	Encaps. Version	P.C.B. Version	Loss in dB at MHz		Pulse and Bar Rating		Box Size*	Encaps. Size*	P.C.B. Size*
					4.43	*3.58*	*kp*	*kpb*			
PAL	2.40/8.18	FRM 443 AB	FRM 443 AE		>38	—	<1%	<4%	A	3	—
PAL	3.68/5.20	FRM 443 BB	FRM 443 BE		>27	—	<2%	<2%	A	1	—
PAL	4.04/4.87	FRM 443 CB		FRM 443 CP	>23	—	<2%	<2%	B	—	C
NTSC	1.94/6.61	FRM 358 AB	FRM 358 AE		—	>38			A	3	—
NTSC	3.00/4.30	FRM 358 BB	FRM 358 BE		—	>27			A	1	—
NTSC	3.37/3.88	FRM 358 CB		FRM 358 CP	—	>23			B	—	C

Technical Data — Pass Filters

TV System	Frequencies at which loss is 3dB *MHz*	Frequencies at which loss is 30dB *MHz*	Box Version	Encaps. Version	Flat Loss in dB at MHz		Box Size*	Encaps. Size*
					4.43	*3.58*		
PAL	4.20/4.60	3.00/7.20	FPM 443 AB	FPM 443 AE	3.00	—	A	2
NTSC	3.40/3.70	2.40/5.80	FPM 358 AB	FPM 358 AE	—	2.00	A	2

* For dimensions see page 11.

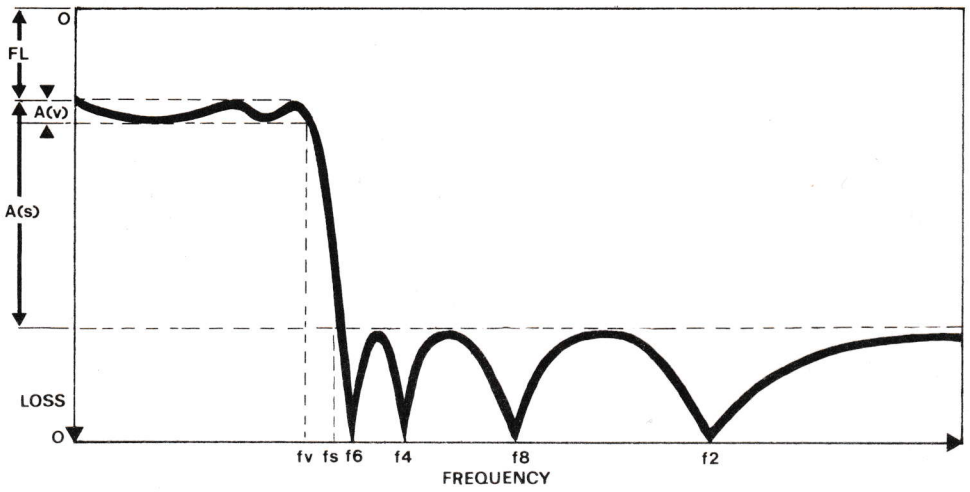
VIDEO FILTERS

Series CFLM, HFM and SFLM Filters

CFLM Series for General Purpose use and for A to D Converters, HFM and SFLM for D to A Converters

The increasing world interest in better TV picture quality via standard analogue systems or via digital TV processing equipment, is creating a need for low pass video filters with both improved and special performances.

The new range of Matthey Low Pass Video Filters has been designed with both these requirements in mind. They have been evolved from the very successful Matthey FLM Series which are in use in television across the world (see page 5).



CFLM Series General purpose and A/D Converter use

The CFLM series are superior in performance to our well-known FLM filters. They are 9 pole 8 zero Elliptic function filters, plus four sections of Group Delay Equalisation and two sections of Amplitude Equalisation which enables us to claim: —

A fast rate of cut-off

Pass band amplitude ripple of less than 0.1dB

Pass-band Group Delay ripple of less than 20ns

Pass-band Return Loss of greater than 25dB

These filters are used in analogue video circuits where excellent performance is desired, and they are also used in A to D Converters where they provide band limitation at the input.

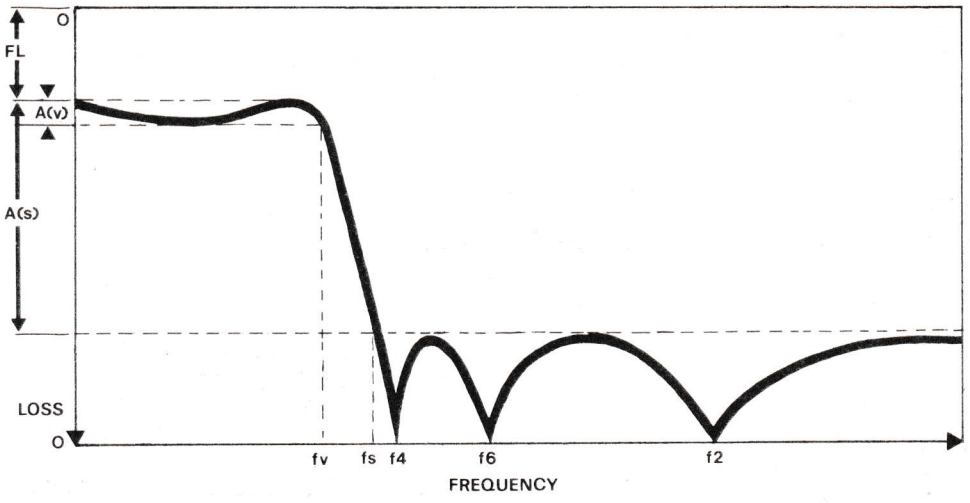
Technical Data—CFLM Series

Model Number	A(s)	Passband Ripple	fs	f2	f4	f6	f8	Group Delay Ripple	Flat Loss(FL) at 100 KHz	Return Loss
	dB	*A(v) (dB)*	*MHz*	*MHz*	*MHz*	*MHz*	*MHz*	*ns*	*dB*	*dB*
CFLM356	> 45	< 0.1 up to 3.2MHz (fv)	3.90	8.68	4.20	3.93	5.11	< 10 to 2.8MHz	0.8	> 26
CFLM410	> 45	< 0.1 up to 4.4 MHz (fv)	5.43	12.09	5.86	5.47	7.12	< 20 to 3.9 MHz	1.6	> 25
CFLM538	> 40	< 0.1 up to 5MHz (fv)	5.76	12.41	6.17	5.80	7.41	< 10 to 4.2MHz	1.1	> 26
CFLM571	> 40	< 0.1 up to 5.2 MHz (fv)	6.00	12.46	6.38	6.03	7.56	< 20 to 4.9 MHz	1.2	> 27
CFLM615	> 40	< 0.1 up to 5.6MHz (fv)	6.58	14.17	7.05	6.63	5.46	< 10 to 4.8MHz	1.1	> 26
CFLM590	> 45	< 0.1 up to 5.7 MHz (fv)	6.46	14.39	6.97	6.51	8.47	< 10 to 4.9 MHz	2.0	> 25
CFLM581	> 40	< 0.1 up to 5.4MHz (fv)	6.15	13.08	6.58	6.20	7.86	< 10 to 4.8MHz	0.9	> 26
CFLM629	> 45	< 0.1 up to 5.9 MHz (fv)	6.88	15.31	7.42	6.93	9.02	< 10 to 5.5 MHz	2.7	> 25
CFLM680	> 45	< 0.1 up to 5.9 MHz (fv)	7.45	16.56	8.03	7.50	9.76	< 10 to 5.4 MHz	0.9	> 25

All the figures are typical.

HFM Series Primarily for D to A Converters, but also for General Purpose use.

These networks have been specially designed for use at the output of D to A Converters. They are 7 pole 6 zero Elliptic Function low pass filters plus three sections of Group Delay Equalisation and one section of Amplitude Equalisation. In two filters the zeros have been designed to occur at the second and fourth harmonics of the colour sub-carrier frequency, thus obtaining maximum rejection of these unwanted signals.



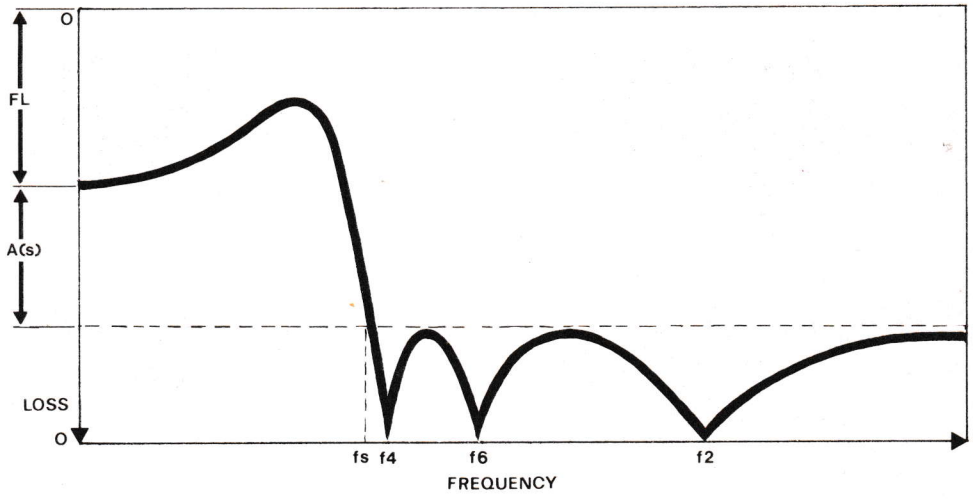
Technical Data—HFM Series

Code	A(s)	Passband Ripple	fs	f2	f4	f6	Group Delay Ripple	Flat Loss (FL) at 100 KHz
	dB	*A(v) (dB)*	*MHz*	*MHz*	*MHz*	*MHz*	*ns*	*dB*
HFM531P	> 45	< 0.2 up to 4.8 MHz (fv)	7.04	14.00	7.16	8.38	< 10 up to 4.8 MHz	0.6
HFM575P	> 45	< 0.1 up to 5 MHz (fv)	7.20	14.78	7.41	8.78	< 10 up to 5.2 MHz	1.8
HFM604P	> 45	< 0.1 up to 6 MHz (fv)	8.70	17.68	8.86	10.50	< 20 up to 6 MHz	0.6
HFM670P	> 45	< 0.2 up to 5.8 MHz (fv)	9.75	22.47	10.00	12.47	< 10 up to 6 MHz	0.6

All the figures are typical.

SFLM Series For use with D to A Converters

These filters are similar to two of the HFM filters and are intended for use at the output of D to A Converters. Their special feature is that Amplitude Equalisers have been incorporated to shape the passband response for sin x/x correction.



Technical Data—SFLM Series

Model Number	A(s)	fs	f2	f4	f6	Group Delay Ripple	Flat Loss (FL) at 100 KHz
	dB	*MHz*	*MHz*	*MHz*	*MHz*	*ns*	*dB*
SFLM488	> 38	7.03	14.29	7.16	8.48	< 30 up to 5 MHz	7.2
SFLM604	> 38	8.70	17.68	8.86	10.50	< 20 up to 6 MHz	6.8

All the figures are typical.

All these filters may be supplied in die-cast boxes fitted with B.N.C. Connectors or as printed circuit board assemblies with flying leads.

For example:—

HFM 575B Die-cast box version (Size B)
HFM 575P Printed Circuit Board version (Size D)

*For dimensions see page 11.

VIDEO FILTERS.

* Millimetre dimensions shown in brackets

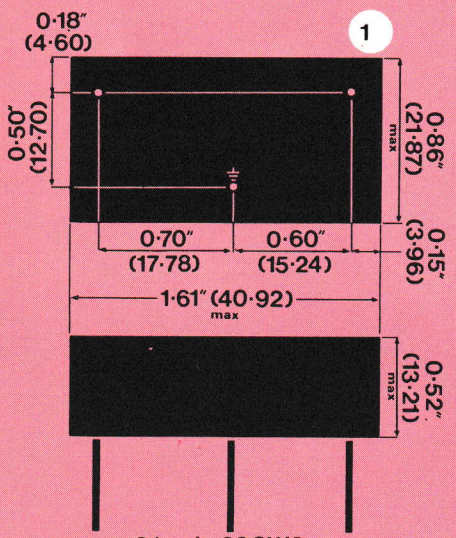
Dimensions

* Lines to pin positions indicate centres

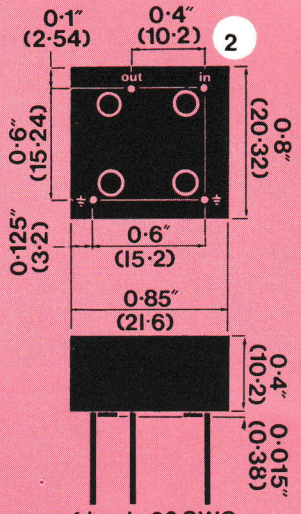
● indicates size number

Box	Length	Width	Height
A	3.63″ (92.20)	1.50″ (38.10)	1.22″ (30.99)
B	4.80″ (121.92)	3.80″ (96.52)	1.20″ (30.48)
PCB	**Length**	**Width**	**Height**
C	4.08″ (103.63)	2.15″ (54.61)	0.90″ (22.86)
D	4.00″ (101.60)	3.12″ (79.38)	0.90″ (22.86)

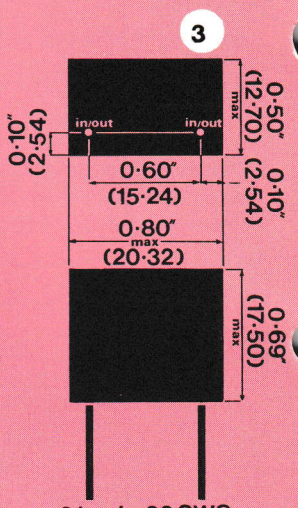
Box dimensions given do not include connectors. (B.N.C. or M.U.S.A. optional).



3 leads 22 SWG
Solder Coated Phosphor Bronze
0·028″(0·700)dia.
0·500″(12·700)long



4 leads 22 SWG
Solder Coated Phosphor Bronze
0·028″(0·700)dia.
0·500″(12·700)long



2 leads 22 SWG
Solder Coated Phosphor Bronze
0·028″(0·700)dia.
0·500″(12·700)long

Filtres vidéo

Dans la télédiffusion en couleurs ou dans la télévision à circuit fermé, on a parfois besoin d'un filtre passif pour résoudre un problème particulier. Souvent, un tel filtre est mis au point par le technicien lui-même, en raison des grands délais pour les unités appropriées peu coûteuses, de bonne qualité. Dans ce fascicule figure la gamme complète des filtres Matthey conçue grâce au concours initial prêté par la British Broadcasting Corporation.

Pour le technicien-studio, les filtres sont fournis avec une impédance de 75Ω et munis de connecteurs BNC pour enfichement rapide dans la route vidéo. Pour les fabricants de matériel, nous fournissons des unités de 75Ω et 510Ω de faibles dimensions, prêtes à être montées sur leurs propres supports ou sur les circuits imprimés.

Nos ingénieurs-vidéo sont toujours disposés à réaliser des modèles particuliers qui ne rentrent pas dans le cadre de ce fascicule.

Видеофильтры

В цветном телевизионном вещании, как и в замкнутых телевизионных системах, часто возникает потребность в светофильтрах для решения особых проблем. Техникам нередко приходится самим изготовлять такие фильтры, поскольку найти такие фильтры удовлетворительного качества и низкой стоимости с быстрой поставкой бывает не легко.

В настоящей брошюре представлен полный сортамент светофильтров, выпускаемых компанией Матти. Мы выражаем признательность Британской радиовещательной корпорации, Би Би Си, за помощь в развитии этой техники, выразившемся в разработке настоящего типажа.

Для студийных техников сообщаем, что эти фильтры имеют сопротивление 75 омов и оснащены разъемами типа "бэби N" для облегчения включения их в контур видеосигнала. Для изготовителей оборудования сообщаем, что оба типа, 75 и 510 омов, выпускаются в виде модуль небольших размеров, готовых для вставления в аппаратурную стойку или печатную плату собственного изготовления.

Специалисты компании Матти готовы спроектировать по заказу фильтры любой спецификации, не включенной в настоящую брошюру.

Video-Filter

Bei derÜbertragung von Farbfernsehsendungen oder bei internen Fernsehanlagen verwendet man häufig passive Filter zur Überwindung spezieller Probleme. Meist konstruiert der Techniker seine eigenen Filter, da passende preisgünstige Geräte guter Qualität selten kurzfristig lieferbar sind.

Der vorliegende Prospekt bahandelt die große Auswahl der Matthey-Filter. Die Entwicklung der Serie erfolgte auf Anregung der British Broadcasting Corporation.

Für den Studioeinsatz liefern wir Filter mit einer Impedanz von 75Ω mit BNC-Anschlüssen zur raschen Einschaltung in den Signalweg. Für den Gerätefabrikanten stehen zwei kleindimensionierte 75Ω und 510Ω Einheiten zum Einbau in eigene Einschübe oder gedruckte Schaltungen zur Verfügung.

Unsere FS-Techniker gehen jederzeit gern auf Sonderwünsche ein, die den Umfang unseres Prospekts überschreiten.

视频滤波器

一般常认为最好用无源滤波器去应对播映彩色电视及CCTV电视时之特殊問題。工程师常决意自设製此种滤波器，因为難覓质好 价廉 且快起货的此种器。

這小册子详細介绍可取用之各齐全种类马瑟滤波器。我们在此答谢英国广播电台之助，致能发展到有這样大量之种类。

为播音室之工程师 備有阻抗75欧姆之滤波器和BNC插头 利便连接視頻信号路線。为仪器製造者，设有面積細小之75欧姆和510欧姆两种单位 可插入他们自有的仪器导軌或印好之电路板。

马瑟滤波器的工程师们，願设计不包括在此册子内之特别部件。

Filtros video

En la difusión de televisión en colores o en televisión a circuito cerrado, muchas veces hay que emplear un filtro pasivo para hacer frente a un problema especial. A menudo, los técnicos mismos deben desarrollar tal filtro, vista la dificultad de hallar un conjunto disponible para la entrega pronta, de buena calidad y precio bajo.

Este librito detalla toda la gama de filtros Matthey. Reconocemos el ayudo de la British Broadcasting Corporation en las etapas iniciales del desarrollo de dicha gama muy extensa.

Para el técnico de estudio, los filtros tienen una impedancia de 75Ω y conectadores BNC para poder enchufarlos rápidamente en la trayectoria de los señales video. Para los fabricantes de equipos, suministramos conjuntos a 75Ω y a 510Ω en pequeñas dimensiones, listos para el montaje en sus propios sostenes o en circuitos impresos.

Los ingenieros video Matthey están siempre dispuestos a idear conjuntos especiales que no sean detallados por el presente librito.

ヴィデオ・フィルター

カラー・テレビ放送(CCTV)では不能動型フィルターを使用して特殊な問題を解決しています。デザイン・エンジニヤーはこのような目的に使うフィルターが低いコストでしかも性能の良いものが欲しい場合に,注文して入手に時間が掛り過ぎるという理由で,それらを自分で作って作ってしまうことがしばしばあります。

このカタログはマッゼー・フィルターのあらゆる型式についてその詳細を記述してあります。このための英国放送協会(BBC)の開発初期の援助が効果的であったために,ここに見るような種々な型式のフィルターが開発された訳で,ここに同協会に対し特に感謝の意を表する次第です。

75Ωインピーダンスを持つフィルター類やBNCコネクター類でビデオ信号回路の接続が容易に出来ることは,スタジオに働いているエンジニヤーにとつて便利な点です。

また,我機製造会社の方々のためには,小型75Ω及び510Ωユニットがあり,部品の枠内や印刷回路板上に簡単に挿入組込めるのです。

マッゼー・フィルター社のエンジニヤーはこのカタログにない特殊型ユニットでも,御要請により,いつでもデザインする用意があります。

Matthey Printed Products Limited

A Johnson Matthey Company

William Clowes Street : Burslem : Stoke-on-Trent ST6 3AT : England

Telex 36341 MPPBUR G: Telegrams+Cables–Matthey Burslem: Telephone–Stoke-on-Trent (0782) 85631

Also ask for data sheets on:

Matthey

Video and Pulse Delay Lines

Chroma Corrector
(puts colour back in its correct place)

Automatic Video Equaliser

Viewfinder Mixer

T.V. Line Selector

Matthey

VIDEO & PULSE DELAY LINES

DELAY LINES·LIGNES A RETARD·DELAY LINES·LAUFZEITKETTEN·LIGNES DE RETARDO·ΔΙΗΝΙΝ ΖΑΕΡΚΗΝ·LINEAS·ヒデオディレーライン·延迟线·DELAY LINES·

1901
July 1975

VIDEO DELAY LINES

In colour television broadcasting precise timing of signals is required. This has been often achieved by installing extra lengths of 75Ω coaxial cable. But, the cost of accurate trimming, plus equalisers, connectors, checking overall performance, and finding space (often under floors) to put the extra cable is steadily increasing.

With initial help from the British Broadcast Corporation Matthey is providing the world TV industry with the largest range of small 75Ω Video Delay Lines, factory tested, and ready to insert into the Colour TV signal path.

They are now used all over the world in studios, outside broadcast units, and CCTV installations. Matthey Delay Line engineers are ready to design special units not included in this catalogue.

PULSE DELAY LINES

For delaying pulses in TV studios for recording, broadcasting or CCTV, low cost delay lines are required having rise times compatible with CCIR Recommendations and having minimum overshoot.

A wide range is described in this catalogue having 240, 270, or 500Ω impedances compatible with active circuitry. In addition, there are many 75Ω delays. The latest product is a ' DO IT YOURSELF ' Delay box (page 15).

- Pour une introduction en votre langue voir la page 24.
- Einführung in Ihrer Sprache siehe S. 24
- Véase página 24 para una introducción en su idioma.
- Введение на Вашем языке на странице 24.
- 第廿四页是用贵国文字写的介绍
- '日本語による御案内は24ページです'

CONTENTS

Video Delay Lines

Pulse Delay Lines


Silver Star
UN 006
equalised VIDEO DELAY LINE
75Ω delay time 1000ns
Matthey
Silver Star
UN 004
Silver Star
UN 068
PULSE DELAY UNIT
75Ω delay time ns
instructions inside box for connecting delay required
Silver Star
UN 360
VIDEO DELAY UNIT
FINE
UN 150
VIDEO DELAY TRIM
UN3/9
3ns-9ns
Matthey
MADE IN UK
7407

VIDEO DELAY LINES

Application Data

The Matthey range of Video Delay Lines (with built in equalisers) is now being adopted by television studios and studio equipment makers throughout the world. The particular advantages compared with 75Ω coaxial cable (the traditional method) are a drastic reduction in size, weight, and installation cost; and a dramatic increase in flexibility of adjustment, and speed of delay time change to suit special event programme requirements.

There are two ranges of Matthey Video Delay Lines to choose from. Studio engineers will find the 5·5MHz range suitable for all studio timing situations. Manufacturers of studio equipments such as mixers (switches) could find the wider bandwidth 10MHz range more suitable especially in designs using signal re-entry—successive re-entry can cause a reduction in bandwidth.

Careful testing of Matthey Video Delays reveals excellent amplitude/frequency response. The overall response is so good that degradation is not observed with normal pulse and bar measurements. (See Photograph 1)

Some of the ways the Matthey Video Delays are used are:

*Studio Timing (See Photograph 2)

*Vision mix units

*Processors

*Coders

*Colour Field Generators

*Other Video Equipments for example the Matthey Chroma Corrector (See Photograph 3)

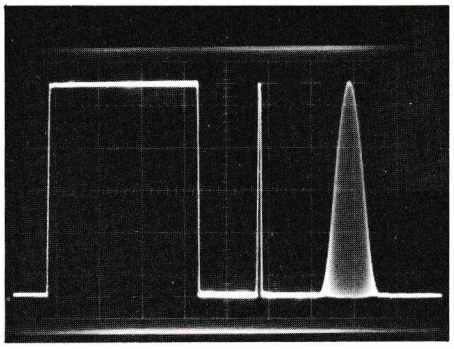
*Installation of studio equipment such as colour camera, Chroma Key unit etc.

*Time base Correctors

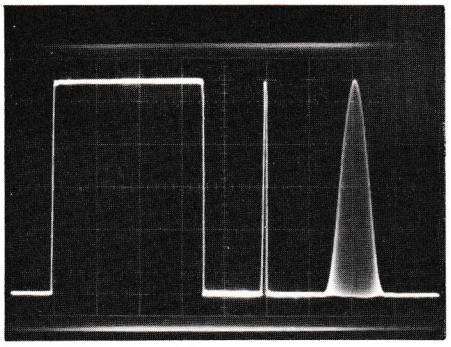
*Outside broadcast units

*University and Industrial TV research

*Teaching in Educational Audio-Visual Departments.



1 **Input**



Output

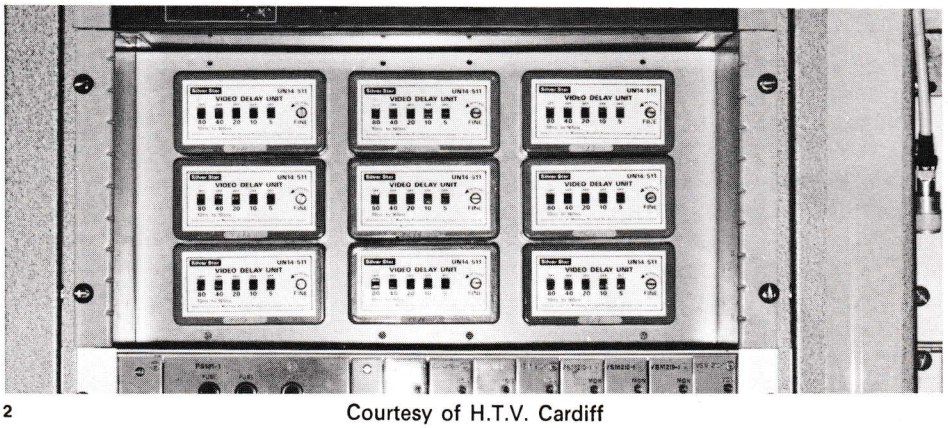
Additional useful benefits, we are informed by users, are:

*Matthey delays have not been subject to attack by vermin as have large coils of coax cables in waterside cellar installations.

*They have small temperature coefficients and small size so the problem of delay change due to hot and cold weather, which can occur to delay cable slung underneath O.B. units, does not occur.

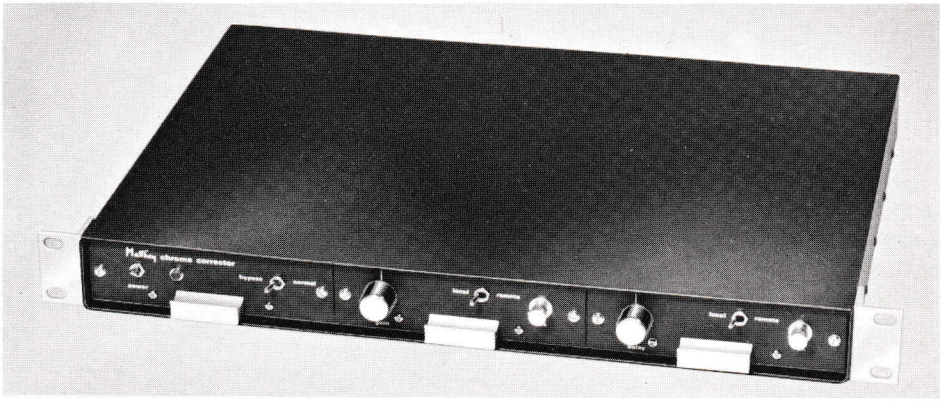
*They have better resistance to change due to humidity.

*They are not subject to aging defects such as the core of delay coax cracking under certain conditions.



2 Courtesy of H.T.V. Cardiff

3



VIDEO DELAY LINES

Series 3·5

Adjustable

These 75Ω delay units (Photograph 4) are designed to fit 19″ equipment racks. They provide bulk delays in a neat compact installation, and give engineers the means of changing the delay time rapidly for special event programmes or to correct for cable variations caused by climatic conditions.

They incorporate the latest Matthey Video Delays giving the best Video performance. Equalisers are built inside so that the unit can be inserted direct into the Video signal path. They are factory tested for Video performance and can be installed without adjustment by the user.

Each unit has an adjustable delay range of 10ns to 165ns (approximately 7ft to 108ft or 2m to 33m of coax.) in 5ns steps by means of switches and a fine trim of ±4ns by screw adjustment. An infinitely adjustable delay is therefore provided.

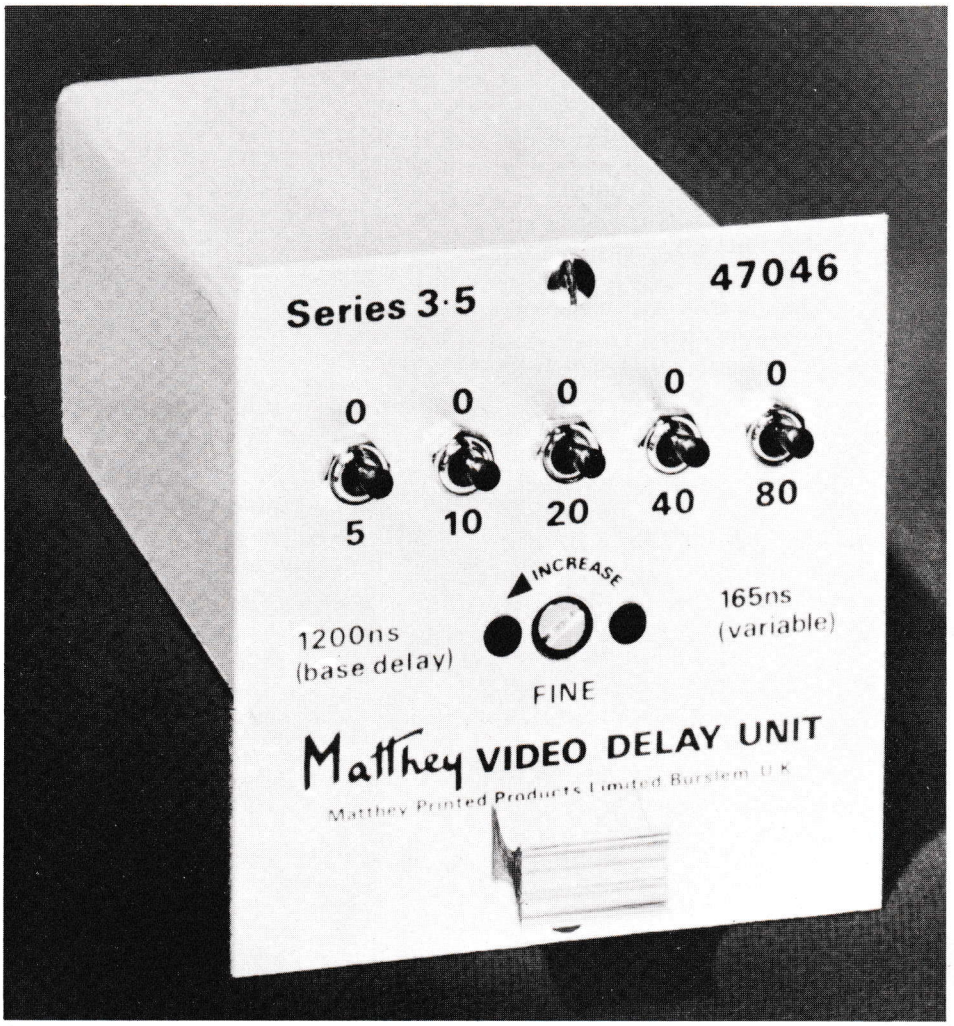
Many users require a 'base' delay in addition to the adjustable part to take the place of long bulky lengths of cable. 'Base' delays from 100ns to 2700ns have already been produced, and we can supply any 'base' delay to suit you.

If you require full adjustment over 360° of phase at colour sub carrier frequency, order 'Series 3·5/360' (Photograph 5). The delay range is 10ns to 325ns—up to 213ft. or 64·94 metres of coax. cable.

Connection to cables is via BNC connectors at the rear. Miniquick and Damar & Hagen connectors can be supplied to order.

Fixed

There are many situations in studio timing where a fixed video delay can be installed to take the place of 75Ω coaxial cable. In these cases a 75Ω 'Series 3·5' fixed Video Delay (Photograph 6) can be provided which fits 19″ equipment racks as do the adjustable ones above.



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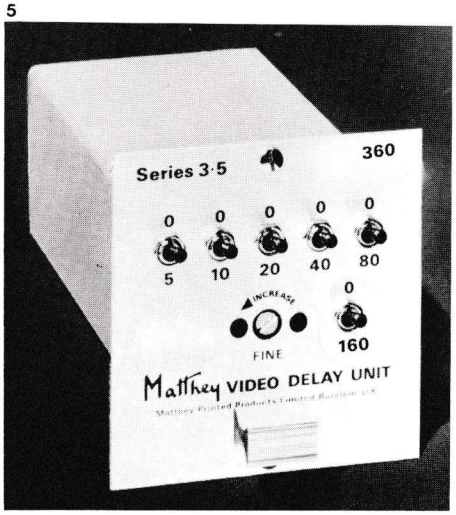
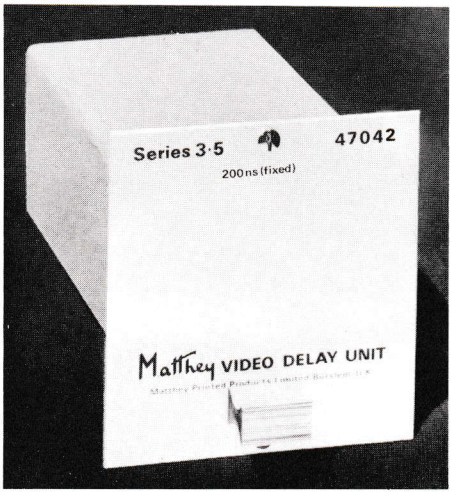


6



Connection is at the back via BNC Connectors. Miniquick, and Damar & Hagen connectors can be supplied to order.

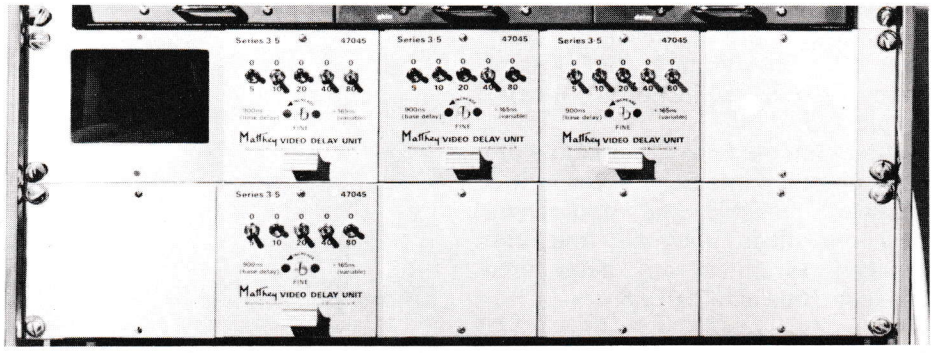
Delay times of 100ns to 2000ns have already been produced. If you require other delay times please ask us.

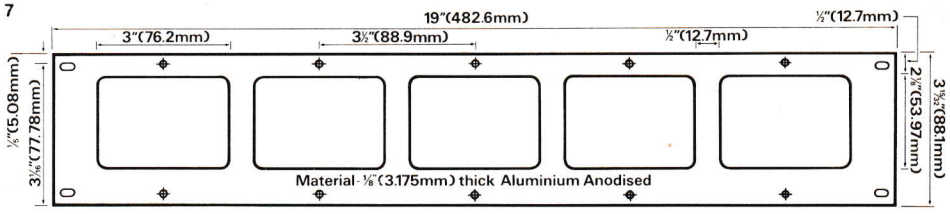
Mounting Panel

The Series 3·5 Video Delay Lines (page 3) are designed to fit 19″ racks. The installation is made easy by the use of 'Series 3·5 Mounting Panels.'

These are made of anodised aluminium and have recesses to take the Delay Lines plus tapped screw holes which match the captive screws on each Delay Unit.

Each 3·5 Mounting Panel can hold up to five fixed or adjustable Series 3·5 units.



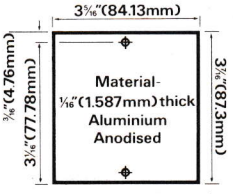


Series 3·5 Mounting Panel

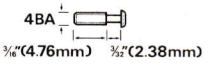
Blanking Panels

For those users who install the 'Series 3·5' Mounting Panel and 'Series 3·5' Video Delays the possibility exists that only three of four units will be installed.

To cover the unused spaces we provide the 'Series 3·5' Blanking Panel fitted with captive screws to make the installation complete and neat.



Blanking Panel



Captive Screw
Brass-Nickel Plate

Technical Data - 3·5 Series

Delay Time *ns*	Model No.	Impedance *Ω*	Flat Loss at 100KHz *dB*	Size
10—165	3·5/47041	75	<0·1	3·44 ×3·31 (Front Panel) ×1·97ins. (87·3 ×84 ×50mm)
10—325	3·5/360	,,	<1·1	
110—265	3·5/47071	,,	<0·5	,,
210—365	3·5/47040	,,	<0·9	,,
310—465	3·5/47050	,,	<1·05	3·44 ×3·31 (Front Panel) ×5·12ins. (87·3 ×84 ×130mm)
410—565	3·5/47044	,,	<1·3	
510—665	3·5/47047	,,	<1·7	,,
610—765	3·5/47048	,,	<1·9	,,
710—865	3·5/47049	,,	<2·05	,,
810—965	3·5/47043	,,	<2·1	,,
910—1065	3·5/47045	,,	<2·2	,,
1210—1365	3·5/47046	,,	<3·6	,,
1810—1965	3·5/47072	,,	<4·8	,,
1910—2065	3·5/47073	,,	<5·0	,,
2710—2865	3·5/47070	,,	<6·4	,,

Finish – Metal Box Anodised Aluminium Front **Operating Temp.** 0 °C to 70 °C **Connectors** – BNC (Miniquick or Damar and Hagen optional)
Other characteristics correspond to those shown for Video P.C.B. Modules on Page 12

VIDEO DELAY LINES

Series 5·25

This new range of Video Delay Line Units fits into a 5·25 inch (13·3 cms) high 19 inch sub rack 'VERO Card Frame Type 3D' 10 inches (25·4 cms) deep.

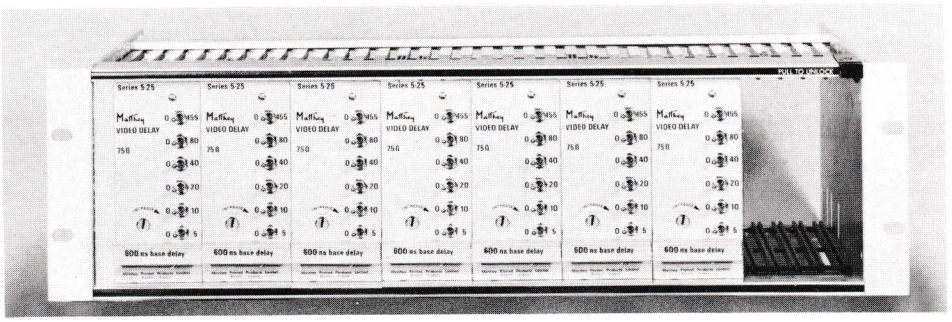
When the modules listed below are fitted on one printed circuit board it is possible, provided the appropriate links are made and the fine trim adjusted, to obtain any delay time between 10ns and 2070ns.

Module No.	Delay Time
47051	5, 10, 20, 40, 80ns
47085	155ns
47086	300ns
47081	600ns
47059	900ns

* See page 10 for technical data.

The nominal delay times shown total 2110ns, but this may become 2070ns when tolerances, delay of trimmer section, and PCB are taken into account.

The special feature of these units is the facility available to the user to alter the delay capability of the unit. Wire links may be soldered to the Printed Circuit Boards to alter the interconnection of modules already fitted, thereby changing the delay time. Also, users who purchase units with less than five modules included may later add extra modules themselves to increase the capability of the unit up to the 2070ns maximum. A wiring diagram is provided.



8

'Series 5·25' Fixed units are supplied with a delay time to order. This delay may be varied ±4ns on the front panel by screwdriver adjustment. 'Series 5·25' switchable units are also produced which provide delay adjustment on the front panel in 5ns steps up to 310ns. A trimmer section of 10ns ±4ns set by screwdriver adjustment is also provided on the front panel.

Seven versions of this style are available as shown below. Each unit ordered will give 320ns of adjustment in addition to a base delay as shown.

As with the non-switch version the user may subsequently increase the 'base' delay if desired by adding extra delay modules from those listed without returning the unit to the Matthey factory.

Provision is made on the PCB for inserting fixed 'T' or π attenuating pads if so desired.

The 'Series 5·25' delay units give the maximum flexibility of choice plus later change if required, for use in constantly changing TV studio situations. To make installation simple, we can supply the complete 19" sub rack unit, which will accommodate up to eight 'Series 5·25' units. Alternatively we can supply 'Series 5·25' units modified to fit other rack mounting systems on request.

Technical Data - Series 5·25

Fixed

Delay Time *ns*	Model No.	Base Delay *ns*	Impedance Ω	Size
To order + Fine Trim	5·25/1	Any delay time between 10 and 2070ns in 5ns steps	75	4·55 × 2·0 (Front Panel) × 8·5ins (incl. switches and BNC connectors) (116 × 50·8 × 21·6mm)
Switchable				
10–320	5·25/2		,,	,,
310–620	,, /3	300	,,	,,
610–920	,, /4	600	,,	,,
910–1220	,, /5	900	,,	,,
1210–1520	,, /6	1210	,,	,,
1510–1820	,, /7	1510	,,	,,
1810–2120	,, /8	1810	,,	,,

Front Panel Finish – Anodised Aluminium **Operating Temp.** 0 °C to 70 °C **Connectors** – BNC mounted on PCB
Total Height of P.C.B. – 4·5ins (114mm)
Other characteristics correspond to those shown for Video P.C.B. Modules on Page 12.

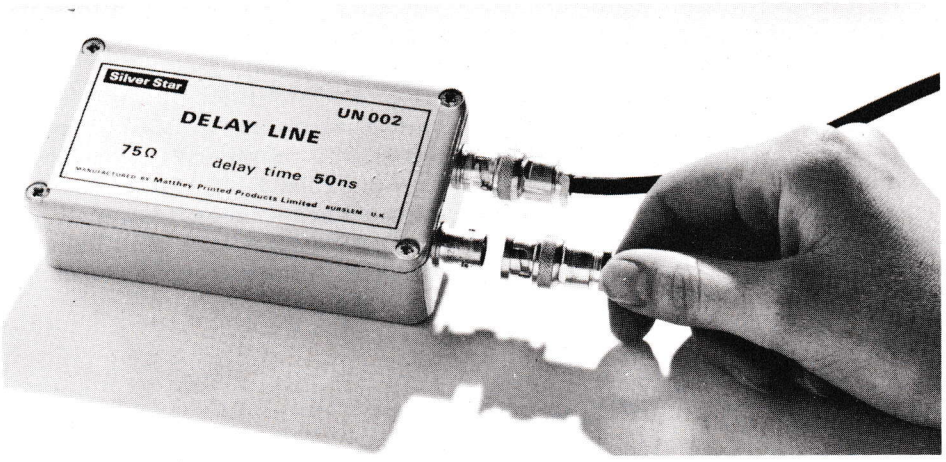
Fixed Boxed Units

The convenience of small 'plug-in' modules instead of long lengths of coax. cable has been regarded as desirable by many engineers, particularly in the field of television broadcasting where full video bandwidth capability is essential.

Now Matthey combines this facility with the high performance standards of Silver Star Video Delay Lines and offer boxed versions fitted with BNC connectors.

Intended for permanent or temporary installation, these robust units are ideal for studio, test, or laboratory work. They can be safely plugged direct into cable runs, thus avoiding the need to make soldered connections or occupy valuable rack space, (for example in providing a Video delay in association with an encoded Chroma Key unit).

Silver Star Video Delay Lines provide accurate delays for 625 line and 525 line colour video signals with minimum distortion and insertion loss up to 5·5MHz. However, the boxed versions are padded out to 3dB ± 0·2dB (with the exception of UN063) for speed of installation with standard 3dB amplifiers. The UN063 has a flat loss not greater than 0·2dB which in most cases is regarded as negligible. Minimum insertion loss versions can be supplied on request.



9

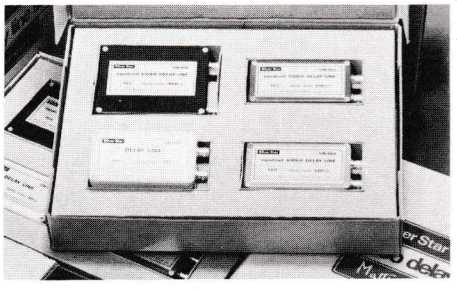
Boxed Sets

This useful new tool has been created at the request of busy Video engineers. Each set contains four 75Ω Video delay lines fitted with BNC connectors. The delay times are 50, 200, 500, and 1000ns, and they can be connected in series to give combinations of these values.

There are numerous occasions when it is necessary to add a Video Delay. 75Ω coaxial cable cut to a specific length and connected via a suitable amplitude equaliser may be used, but this method demands a large amount of space and is time consuming for the engineer to design and install.

The Silver Star Video Delay Lines are fully amplitude equalised, and are ready to use. The equalisers are built inside the units. They can be used for timing a new Video route quickly without using long lengths of cable. They can then be left as a permanent installation or replaced later by the smaller Silver Star Delay Line modules on printed circuit boards if preferred. (see page 9).

10



Technical Data - Video Fixed Boxed Units

Delay Time *ns*	Model No.	Tolerance *ns*	Impedance *Ω*	Flat Loss at 100KHz *dB*	Approx. Weight *gms.*	Size
50	UN063	+4–0	75	<0·1	148	4·37 ×2·37 ×1·22ins (111·1 ×60·3 ×31·0mm)
100	UN023	±5	,,	3±0·2	168	,,
200	UN005	±5	,,	,,	168	,,
300	UN069	+0–15	,,	,,	206	,,
500	UN004	+0–15	,,	,,	206	,,
1000	UN006	+0–25	,,	,,	337	4·75 ×3·75 ×1·16ins (120·6 ×95·2 ×29·4mm)

Finish – Die Cast Metal Box **Operating Temp.** 0 °C to 70 °C **Connectors** – BNC (Miniquick or Damar and Hagen optional)
Other characteristics correspond to those shown for Video P.C.B. Modules on Page 12.

VIDEO DELAY LINES

Variable Boxed Units

UN360

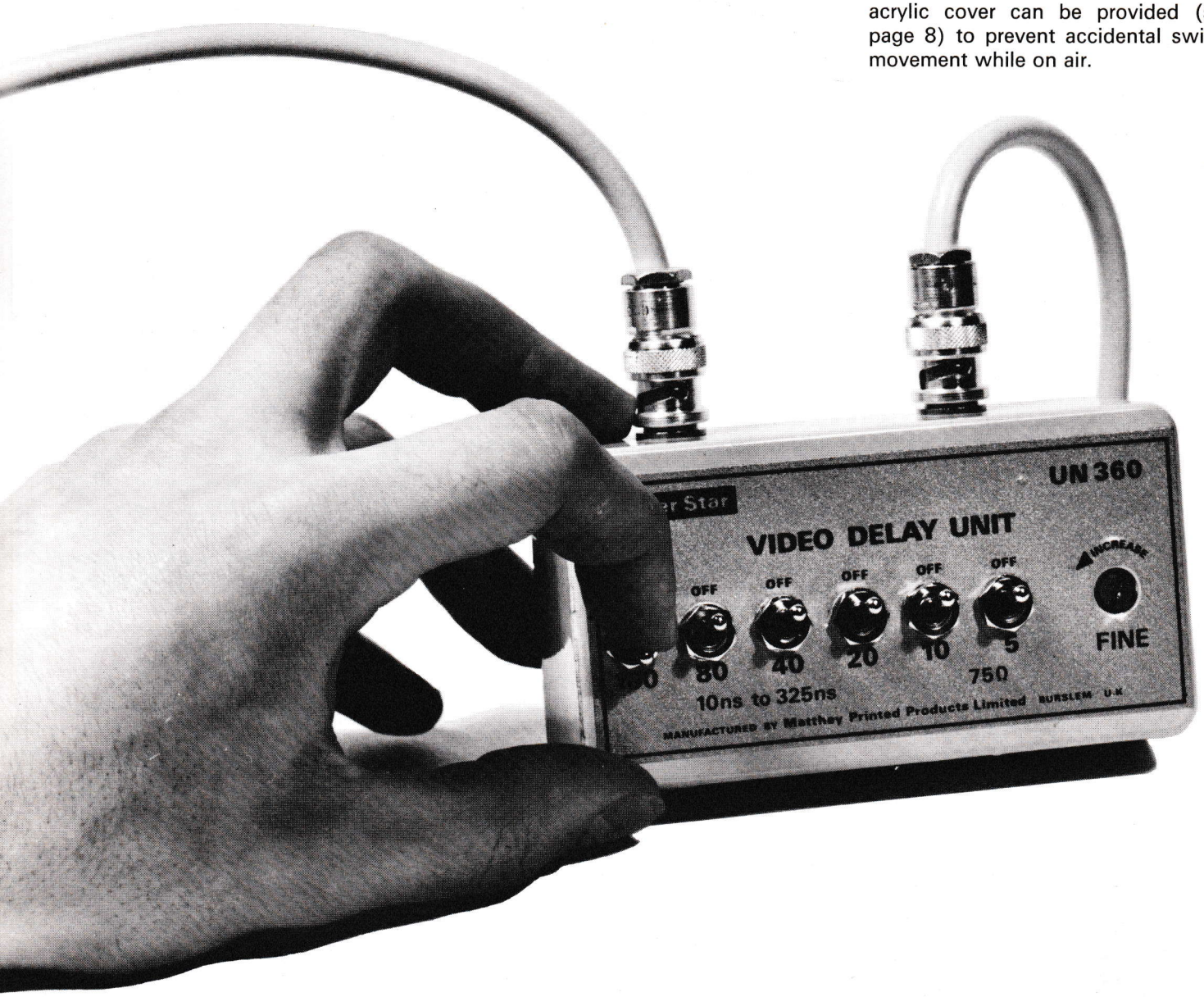
Video engineers often require to vary the phase of the colour sub carrier quickly and accurately. The 'Silver Star' Video Delay Unit UN360 is designed to phase shift the colour sub-carrier between 16° and more than 360°.

360° PAL sub carrier	=225·5ns
360° NTSC sub carrier	=279·4ns
360° SECAM sub carrier	=225·5ns

In all cases the UN360 can delay beyond 360° phase with its maximum delay of 325ns.

Six switches allow delays to be selected between 10ns and 325ns in 5ns steps. A screwdriver setting of the trimmer provides a continuously variable adjustment of ±4ns. Amplitude equalisation of the 20, 40, 80 and 160ns delay sections ensures a good amplitude response shape.

The UN360 is intended for use primarily with colour television mixing equipment to facilitate rapid and precise timing for specific special event programmes. Its performance is such that it may also be used as a long term installation in Video circuits. A clear acrylic cover can be provided (see page 8) to prevent accidental switch movement while on air.



UN180

Based on a British Broadcasting Corporation specification, Silver Star Video Delay Unit UN180 offers rapid and accurate selection, by means of switches, of any delay time from 10ns to 165ns with fine trim of ±4ns by screw adjustment.

Like other video delay lines in the Silver Star range, unit UN180 is designed for colour working.

The unit is intended for use primarily with colour television vision mixing equipment to facilitate rapid and precise timing on a temporary basis for specific, special event programmes.

Both video delay unit UN180 and UN360 can be cascaded with the 50ns, 200ns, 500ns and 1000ns fixed delay units. The fixed delay units can also be cascaded with each other to provide delays of up to 4μs.

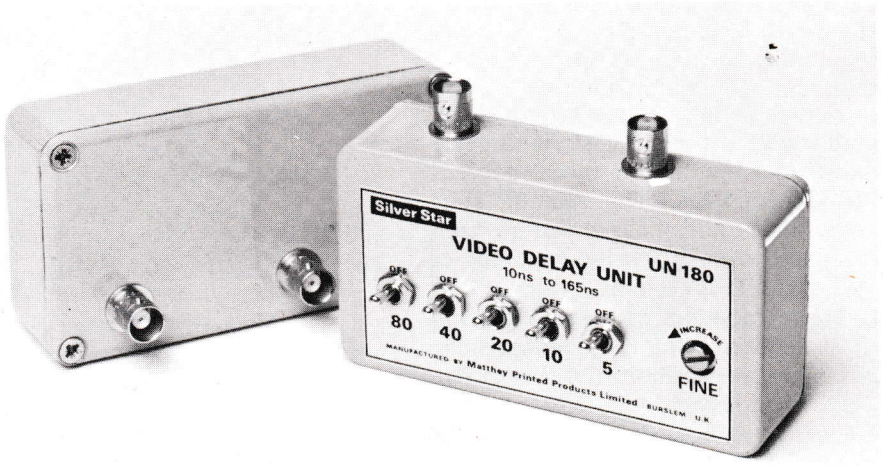
Model 'UN180 Rear Mounted' is also available with BNC connectors fitted at the back instead of the top.

Acrylic Cover

This transparent delay unit cover is designed as a push fit on to the unit to protect the switches from accidental movement during a T.V. programme transmission.

It is interchangeable with either unit UN180 (10ns to 165ns) or unit UN360 (10ns to 325ns).

The design gives a firm protection against switch movement, but the cover can be quickly and easily removed when a delay time change needs to be made. It should be specified separately on your order.



12

UN3/9

A constant problem in TV studios is the trimming of delay times due to the difficulty of cutting coaxial cable to the exact length required. Even if exact lengths are used, drift due to temperature change can still occur.

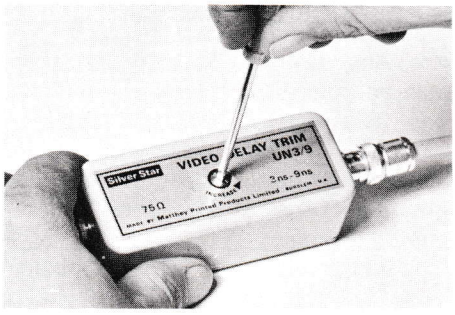
The unit UN3/9 is designed to be a low cost insert into cable runs to provide a continuous variation over 6ns (equivalent to 120cms or 4 feet of cable).

There is no significant distortion to the video signal and insertion loss is less than 0·15dB up to 5·5MHz.

The design impedance is 75Ω to make it instantly useable in studios, OB units and laboratories.

13

14



Technical Data - Video Variable Boxed Units

Delay Time *ns*	Model No.	Impedance *Ω*	Flat Loss at 100KHz *dB*	Approx. Weight *gms.*	Size
3–9	UN3/9	75	<0·1	103	3·56 ×1·5 ×1·25ins. (90·5 ×38·1 ×31·8mm)
10–165	UN180	,,	<0·1	210	4·5 ×2·5 ×1·25ins. (114 ×63·5 ×31·8mm)
10–325	UN360	,,	<1·1 (At Max. Delay)	240	4·5 ×2·5 ×1·25ins. (114 ×63·5 ×31·8mm)

Finish – Die Cast Metal Box **Operating Temp** 0 °C to 70 °C **Connectors** – BNC (Miniquick or Damar and Hagen optional)
Other characteristics correspond to those shown for Video P.C.B. Modules on Page 12

VIDEO DELAY LINES

Printed Circuit Board Modules

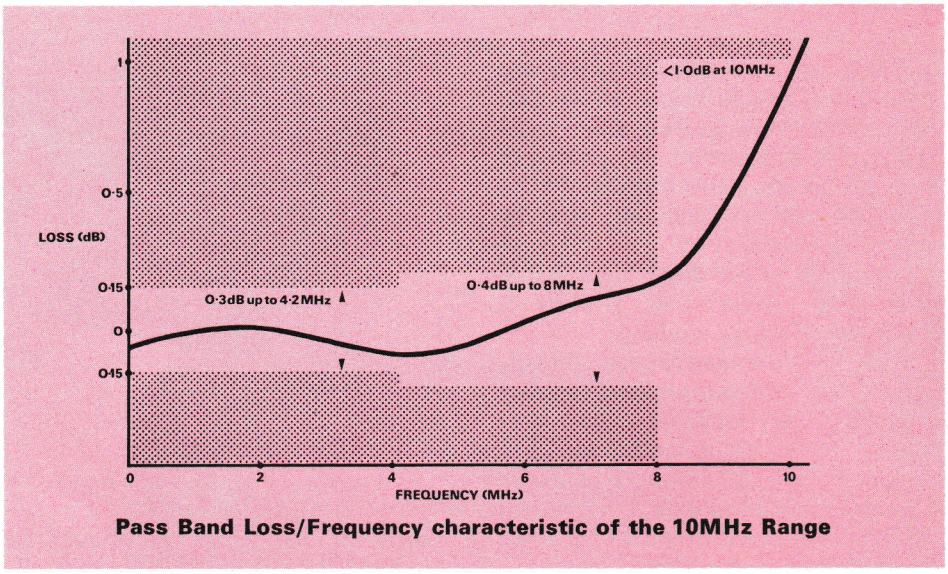
Programmable - 5·5MHz

Sub Carrier Delays

Colour television broadcasting engineers need, on occasions to delay sub-carrier frequencies by 90 degrees or 180 degrees. The Colour sub-carrier delay lines have therefore been designed to meet the requirements of PAL and NTSC systems.

These modules consist of a main delay section giving the nominal delay required. In addition there are five sections providing ½, 1, 2, 2, and 4ns respectively, thus enabling series connections to be made to achieve an accurate setting in circuit.

The main delay section is amplitude equalised.



Pass Band Loss/Frequency characteristic of the 10MHz Range

47058 Trimmer (0·5ns - 9·5ns) 5·5 and 10MHz

This 75Ω trimmer delay module has been specially designed to replace the short lengths of 75Ω delay cable that are often cut and installed in Video equipment to adjust delay times to fine limits.

Five separate delays are provided in the one module: ½ns, 1ns, 2ns, 2ns, 4ns. Any combination of these delays may be connected giving approximate ½ns delay steps between ½ns and 9½ns. It is, therefore, very easy to install this dual-in-line unit and have great flexibility of fine delay adjustment available.

Manufacturers of video mixers/switchers will find this Trimmer Delay occupies minimal space. This will also be of importance in outside broadcast (remote) vans, miniature colour cameras, and any other equipment where space saving plus ease of time adjustment is desired.

The Trimmer Delay can be cascaded with other 'Silver Star' Pulse or Video delay lines to give longer but finely trimmed delays.

47051 (5ns - 155ns)

This delay line has been designed to provide 75Ω delay from 5ns to 155ns in increments of 5ns.

Five separate delays of 5ns, 10ns, 20ns, 40ns, and 80ns, are included together with equalisation circuits to maintain a good amplitude response, irrespective of the delay time selected.

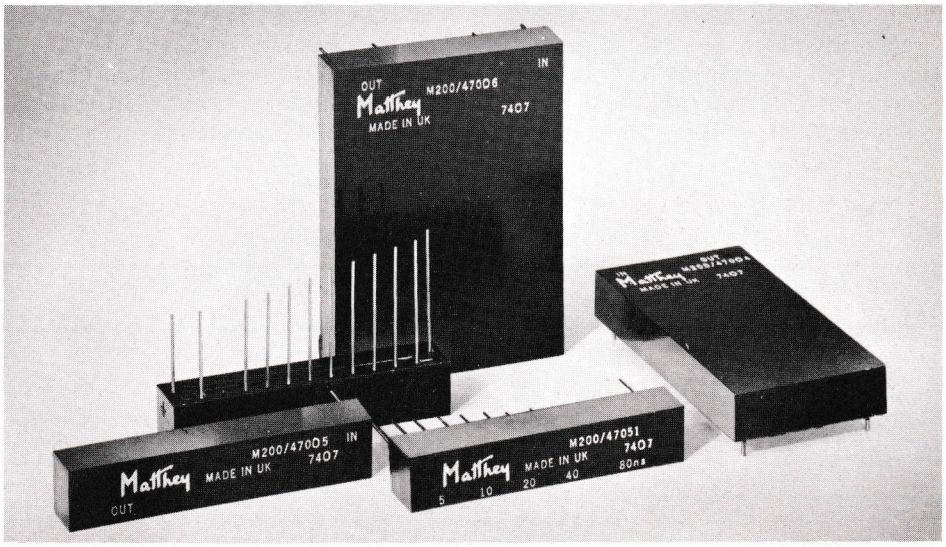
It is particularly suitable for connecting in series with the other 75Ω 'Silver Star' equalised Video Delay Lines.

47022 (5ns - 35ns)

There are many applications on printed circuit boards where the full range of module 47051 (5 to 155ns) is not required. For this reason we have module 47022 available with a range 5ns – 35ns in 5ns steps. The benefits to the user are smaller size and lower price.

47067 (5ns - 235ns)

To suit certain customers we have designed this variation of module 47051. The delay range has been increased to 225ns without increasing



the module size. Delay may be selected in 5ns steps from 5–225ns. Equalisers are built inside to provide a good amplitude/frequency response.

Fixed - 5·5 & 10MHz

Matthey 'Silver Star' Video Delays are the world's most compact self contained equivalents to 75Ω coaxial cable. Unlike coax. they contain their own equalisers and are factory tested ready for use up to 5·5MHz. These modules provide bulk delays. Fine adjustments of delay can be obtained by also using 'Programmable' delays described on these pages.

Equipment designers will find the 10MHz fixed delay lines useful especially where signal re-entry is a function of the equipment design. The amplitude frequency response is controlled to give a broadcast quality performance from low frequency up to 10MHz. The specification for ripple control is shown in the diagram. The flat loss for each delay module is shown in the table. They can be used separately or in cascade to form longer delays.

Technical Data - Video P.C.B. Modules

Programmable 5·5MHz

Delay Time *ns*	Module No.	Tolerance *ns*	Delay per Section *ns*	Impedance *Ω*	Flat Loss at 100KHz *dB*	Approx. Weight *gms.*	Size
90° Pal Sub Carr.	47054		to within 0·5ns.	75	<0·30	14·0	5a
180° Pal Sub Carr.	47055		,,	,,	<0·40	23·0	3b
90° NTSC	47056		,,	,,	<0·40	14·0	5b
180° NTSC	47057		,,	,,	<0·50	23·0	3a
360° Pal & NTSC	47066		,,	,,	<1·20	70·0	2a
0·5–9·5	47058		0·5ns steps	,,	<0·05	4·5	7
5–155	47051		5ns steps	,,	<0·65	20·0	6a
5–235	47067		5ns steps	,,	<0·90	25·0	6b
Fixed 5·5MHz							
50	47063	+4–0		,,	<0·10	20·0	4
100	47023	±5		,,	<0·45	25·0	4
155	47085	±3		,,	<0·50	25·0	4
160	47062	±5		,,	<0·50	25·0	4
200	47005	±5		,,	<0·80	25·0	4
300	47086	+10–5		,,	<0·90	70·0	2b
400	47029	+0–15		,,	<1·00	70·0	2b
500	47004	+0–15		,,	<1·60	70·0	2b
600	47081	+0–20		,,	<1·60	70·0	2b
800	47028	+0–25		,,	<2·00	100·0	1
900	47059	+0–25		,,	<2·60	100·0	1
1,000	47006	+0–25		,,	<2·70	100·0	1
Fixed 10MHz							
50	47032	+4–0		,,	<0·10	25·0	4
100	47033	±5		,,	<0·50	25·0	4
200	47035	±5		,,	<1·00	25·0	4
300	47030	±5		,,	<1·00	70·0	2b
400	47031	+0–15		,,	<1·30	70·0	2b
500	47034	+0–15		,,	<1·75	70·0	2b
1,000	47036	+0–25		,,	<3·50	100·0	1

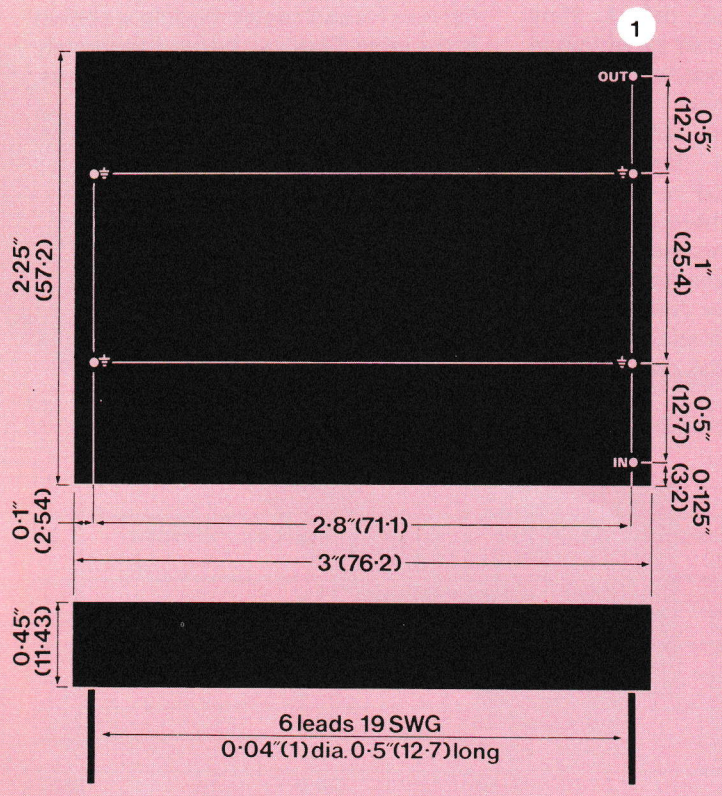
For general data and dimensions see Page 12.

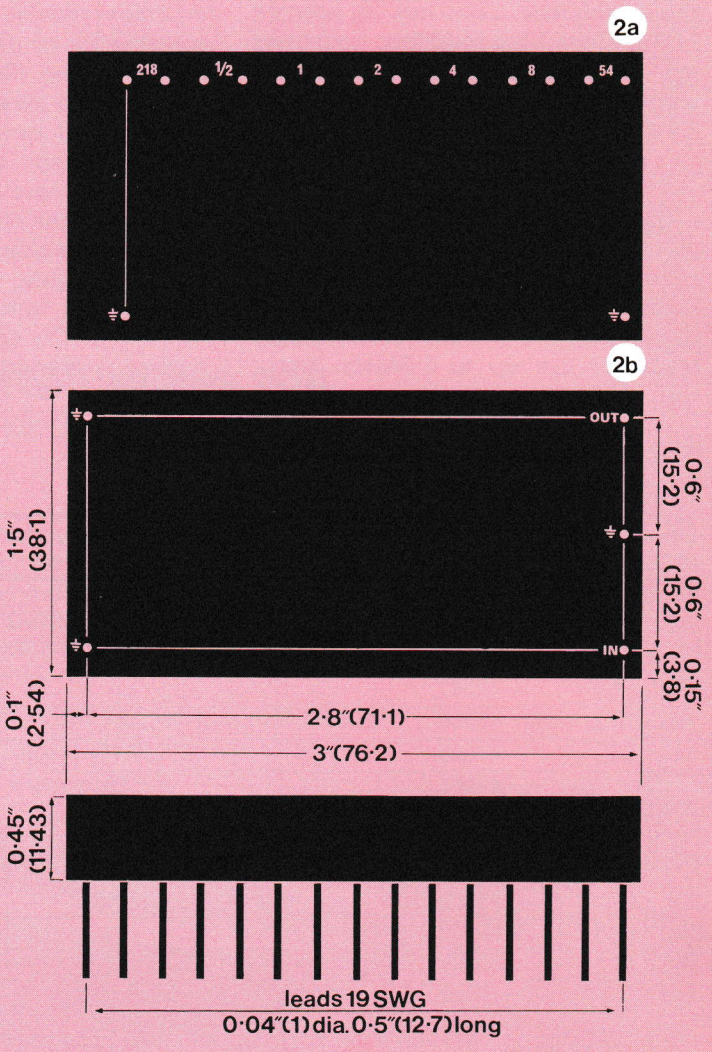
VIDEO DELAY LINES

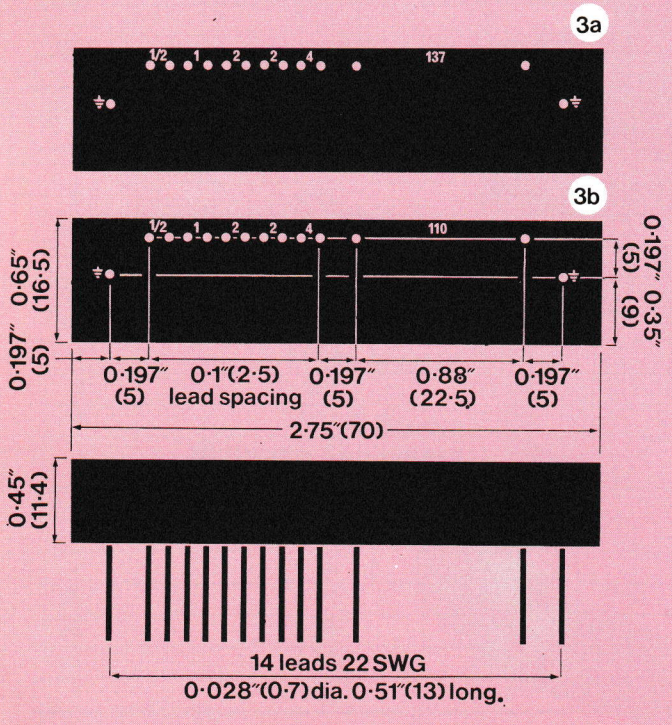
Dimensions & General Data - PCB Modules

● indicates size number

* Small figures within the modules show delay times (ns)
* Lines to pin positions indicate centres
* Millimetre dimensions shown in brackets





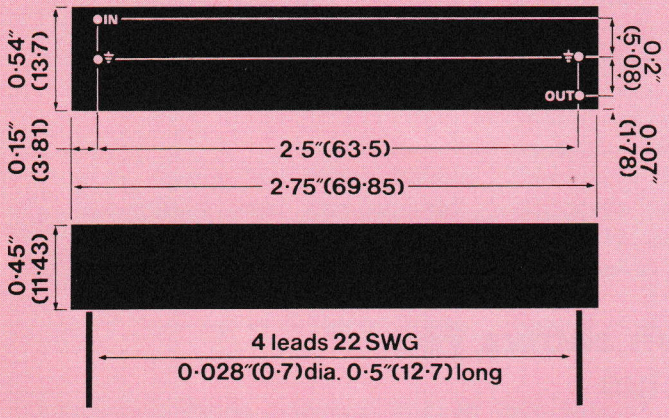


General Data - Video P.C.B. Modules

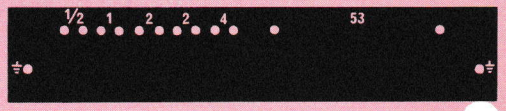
Amplitude/Frequency Response	(a) Loss at 4·43MHz relative to 100 KHz ±0·1 dB *(b) Ripple up to 5·5 MHz <0·2 dB (c) Module 47063 Loss at 5·5 MHz <0·15 dB
Return Loss	Greater than 20dB up to 5·5 MHz
Temperature Coefficient	Pulse Delay ±0·1ns/μs/deg. C.
Temperature Range	–55 °C to 100 °C
Maximum Input Voltage	5 V.d.c.
Finish	Synthetic Resin Encapsulated
Pins	Solder Coated Phosphor Bronze

*Ripple up to 10 MHz:
0·3dB up to 4·2 MHz
0·4dB up to 8·0 MHz
<1·0dB at 10 MHz

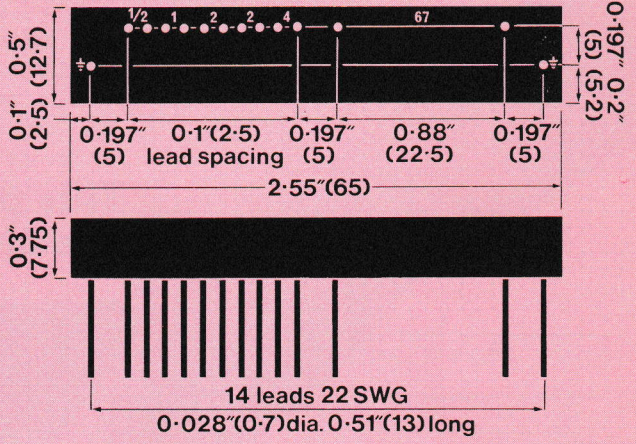
4



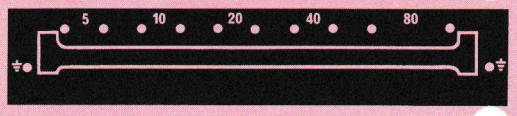
5a



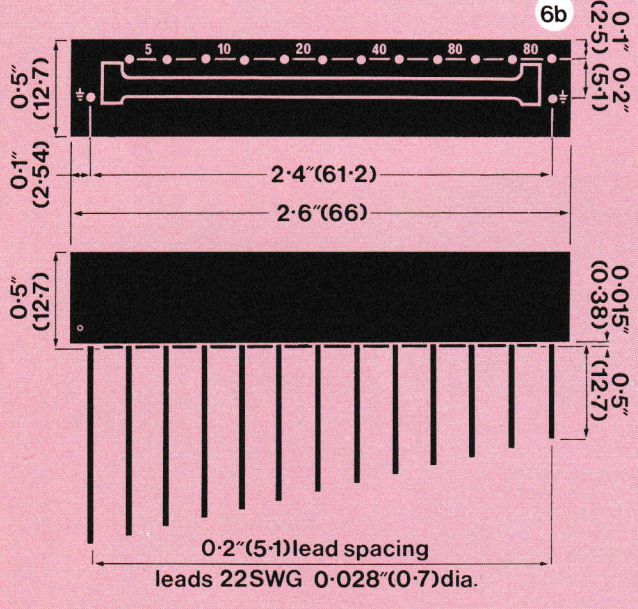
5b



6a



6b



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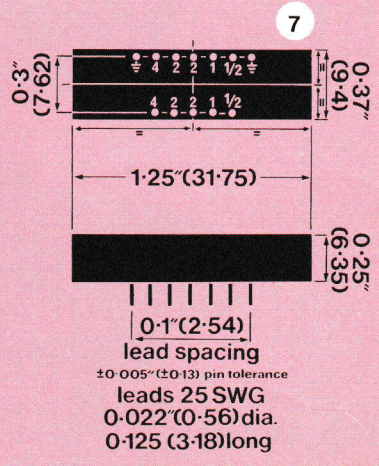
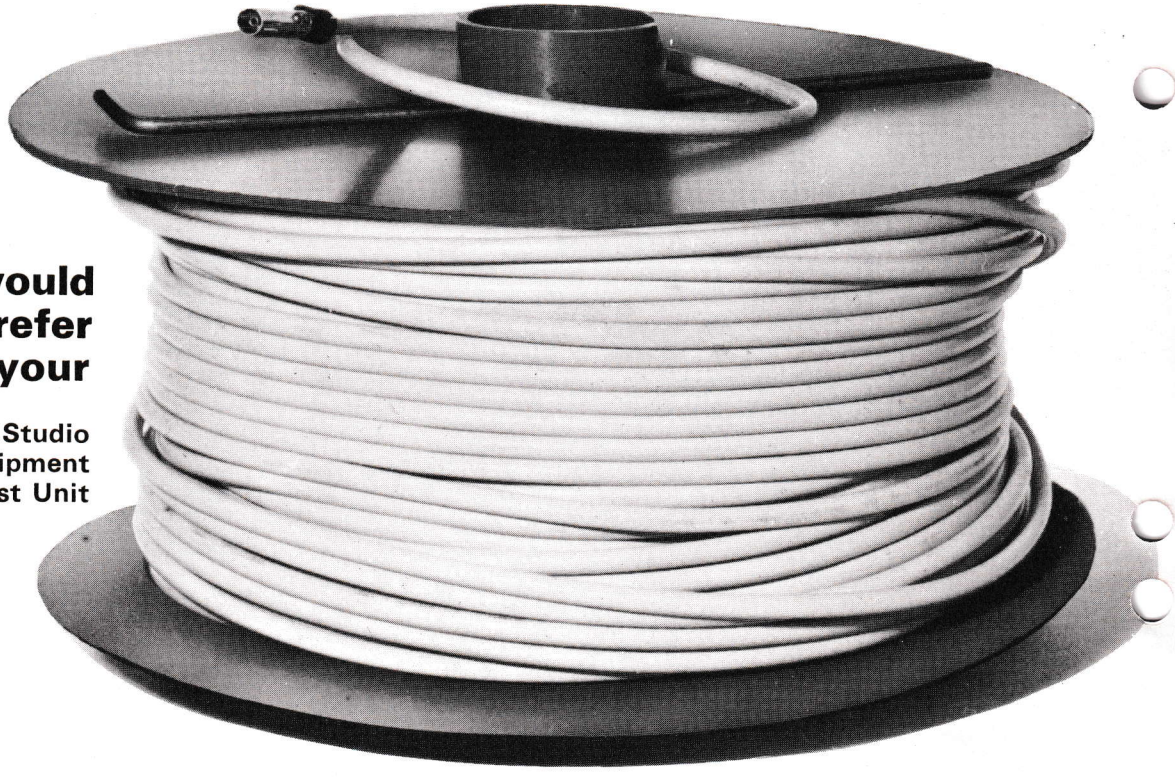


75Ω Coaxial Cable or

Matthey DELAY

This photograph shows you the choice for 1μs

One Delay Module 47006
Weight: 100 gms. (0·22 lbs.)
or
650 ft. (200 m.) of Coaxial Cable
Weight: 20 kgs. (44 lbs.)



Which would you prefer in your

- Studio
- Studio Equipment
- Outside Broadcast Unit

PULSE DELAY LINES

Application Data

The ways of delaying composite Video signals are dealt with in the first half of this catalogue.

In addition, studios rely on synchronising pulse trains to bring all on line equipment within the TV station to within about 50ns for monochrome broadcasting, and to within about 20ns for colour broadcasting. For these applications we recommend a 'Silver Star' PULSE Delay Line. They are lower in cost but they are still made to extremely high standards.

CCIR recommendations for synchronising pulses in 525 line and 625 line broadcasting state a rise time of 250ns ±50ns with an overshoot of less than 5%.

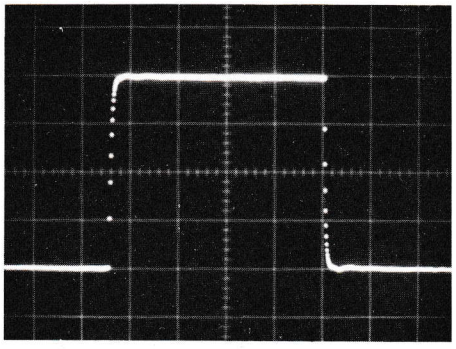
The Silver Star pulse delay lines in this catalogue are all compatible with that requirement. The performance may best be seen in the photographs below, showing the output from a typical Silver Star PULSE delay line.

The Matthey range provides many modules with 75Ω impedance. For users requiring to include delays in active circuitry the modules with impedances of 240Ω, 270Ω or 500Ω will be useful.

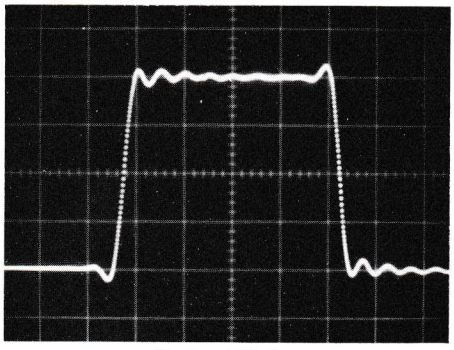
In studio equipment almost any combination of printed circuit board modules is possible providing delay times from 0·5ns to 4500ns without sacrificing CCIR recommended rise times.

When installing new studio equipment some retiming is usually necessary due to the inherent delays contained in the new equipment. These delay times are known approximately at the time of ordering the equipment. The final delay time may not be decided until the moment of installation. For this situation we have designed the 'DO IT YOURSELF' Pulse Delay Unit UN068 (see page 15).

16 **Typical Pulse Response of delay line 47014 (Delay Time 1500ns)**

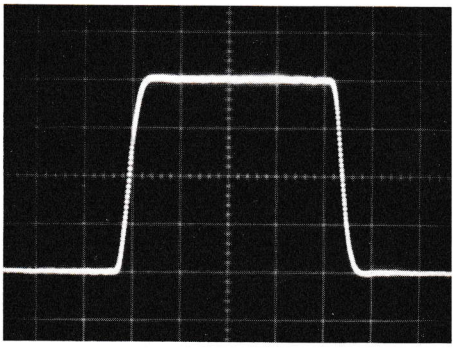


Input Pulse
Rise Time 1ns

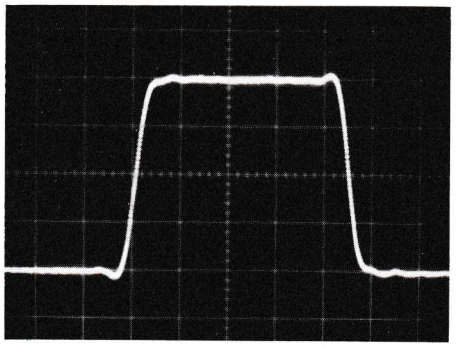


Output Pulse
Rise Time 155ns Overshoot <5%

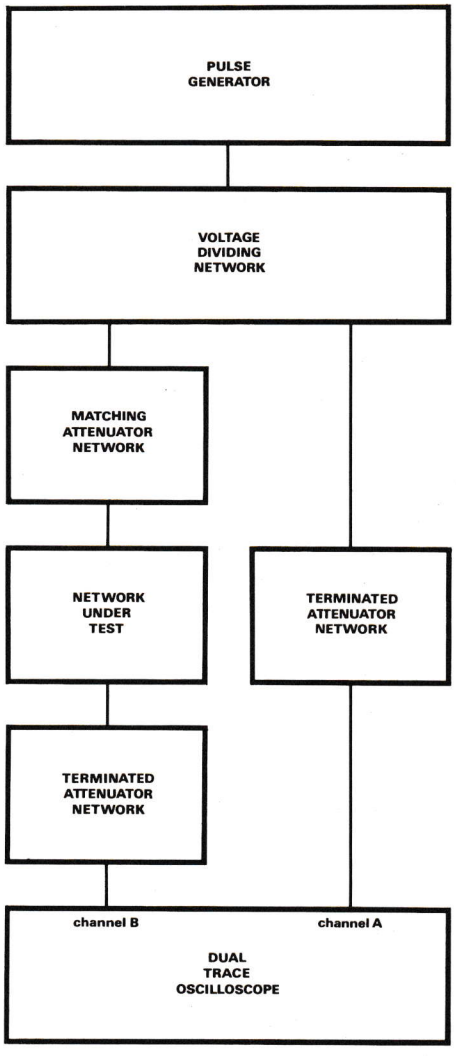
Input Pulse
Rise Time 170ns



Output Pulse
Rise Time 210ns Overshoot negligible



Because of the different methods available for measuring delay times accurately we recommend either the use of specialist equipment or a test circuit based on the following:



The attenuator matching pads etc., necessary to terminate the network correctly and minimise the effects of reactances, would normally be located in a test jig. All leads should be as short as possible and the resistors should have adequate frequency response characteristics.

PULSE DELAY LINES

UN068

Video engineers often need to delay 75Ω timing pulses for periods ranging from a few nanoseconds to several microseconds. Once the delay time has been determined for a particular part of the circuit a fixed delay line can be installed. An expensive switched delay line is therefore neither necessary nor desirable.

The 'Pulse Delay Unit UN068' has been designed specifically for this application. It can be supplied in two versions; either to give a delay time between 5ns and 3155ns in 5ns increments, or to give delay times between 100ns and 4500ns in 100ns increments.

The unit is normally supplied unconnected internally so that an engineer may select and connect the delay time he requires. This method gives freedom for a last minute change of delay time. A wiring diagram is inside each unit to facilitate this.

If preferred the unit UN068 can be supplied with a specific delay time connected ready for use.

Method

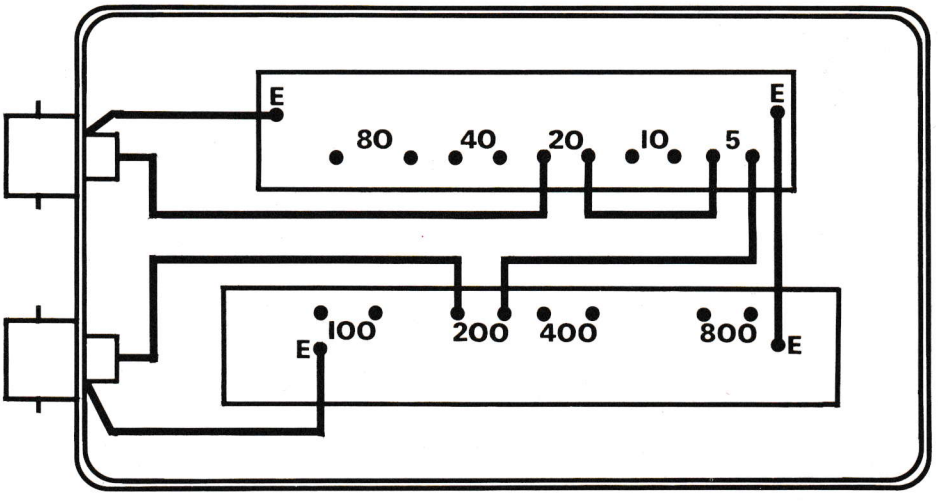
1. Order UN068 and state approximate delay time and delay steps required.

Example:

(a) UN068 1100ns (100ns steps)
(b) UN068 1500ns (5ns steps)

2. Remove lid and connect delay required.
3. Replace lid and use as fixed delay.

Note: For delaying composite colour video signals in television broadcasting without significant distortion use Matthey Video Delays (see pages 6,7 & 8).



Example for wiring 225ns

Technical Data - UN068

Delay Time *ns*	Impedance *Ω*	Rise Time at Max. Delay *ns*	Delay Steps *ns*	Approx. Weight *gms.*	Size
5–155	75	<35	5	185	4·5 × 2·5 × 1·25ins. (114 × 63·5 × 31·8mm)
160–1655	,,	<180	,,	,,	,,
1660–3155	,,	<210	,,	,,	,,
100–1500	,,	<180	100	,,	,,
1600–3000	,,	<210	,,	,,	,,
3100–4500	,,	<250	,,	,,	,,

Finish – Die Cast Metal Box **Operating Temp.** 0 °C to 70 °C **Connectors** – B.N.C. (Miniquick or Damar and Hagen optional)
Other characteristics correspond to those shown for Pulse P.C.B. Modules on Page 22

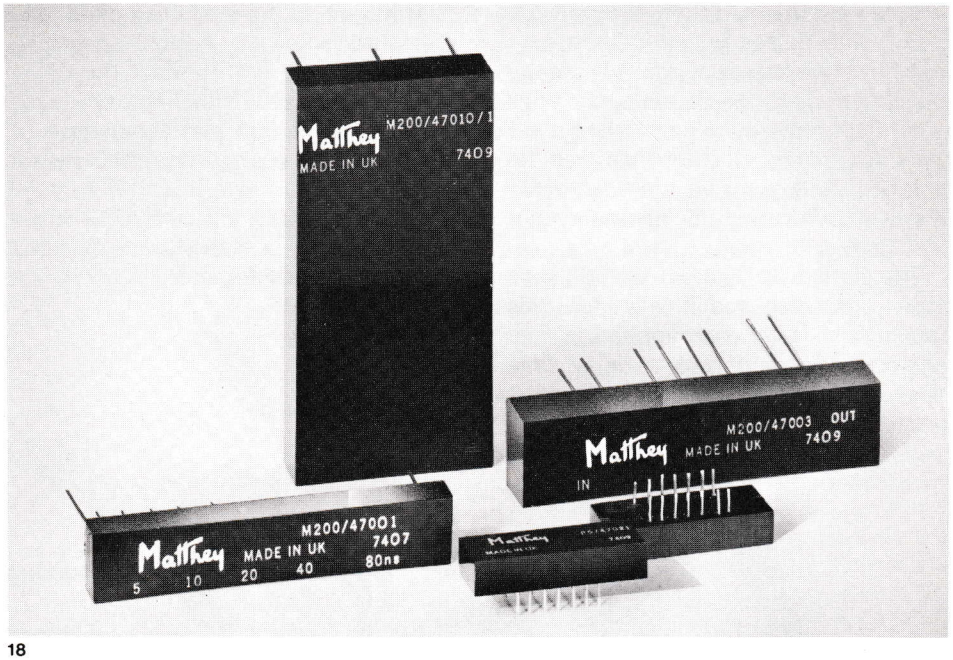
PULSE DELAY LINES

Printed Circuit Board Modules

'Silver Star' Pulse Delay Lines are Lumped Constant (LC) units designed for use in Television Broadcasting Equipment. In their manufacture we use the well known 'professional' grade 'Silver Star' mica capacitors, which ensures high reliability and long term stability.

Note the small temperature coefficient of delay: $\pm 0{\cdot}1\text{ns}/\mu\text{s}/^{\circ}\text{C}$

All programmable Delays can be terminated at whatever delay time is required without causing unwanted reflections from the end of the line.



18

Programmable

47058 Trimmer (0·5ns - 9·5ns)

This module provides delays in 0·5ns steps from 0·5ns to 9·5ns. Whilst such fine adjustment is not normally required for pulses in studios, nevertheless equipment manufacturers are interested for making their equipment as closely timed and controlled as possible. It can be connected in series with other pulse delay lines without significantly affecting the pulse shape.

47001 (5ns - 155ns)

This module provides slightly larger increments of 5ns each, from 5ns to 155ns. The performance of this delay is very good and has resulted in its being designed into studio equipments of all kinds in many parts of the world.

In manufacture particular care is taken over the matching of adjacent sections so that mismatch does not occur in any significant way. This is so even when the delay sections used are remote from each other – for example 5ns + 80ns.

47022 (5ns - 35ns)

This module is designed to be fitted into studio equipment when the full delay range of 47001 (5 – 155ns) is not required.

By eliminating the longer delay times it is possible to provide not only a cheaper module but a smaller one. This delay is made to the same high standard of performance and is widely used either alone or in series with others of the 'Silver Star' Pulse Delay Lines.

47083 (20ns - 620ns)

Also a 75Ω module which gives a binary progression of separate delays 20, 40, 80, 160, 320ns. Therefore, any delay time between 20 and 620ns can be connected at increments of 20ns.

47014 (100ns - 1500ns)

The continuous expansion and extension of existing studios is creating a need for far greater lumps of delay for timing of pulses.

The 47014 module provides separate 100, 200, 400, and 800ns delay sections in one unit. Any combination can be connected in series without fear of reflections from the end of the module. It is, therefore, possible to achieve a delay of 100ns, or multiples of 100ns, up to a maximum of 1500ns.

If times longer than 1500ns are required, up to three modules can be connected in series (4500ns maximum) without sacrificing rise time and overshoot limits as recommended by CCIR.

47061 (25ns - 175ns)

This 75Ω delay gives another choice to equipment designers where seven 25ns steps are provided, giving either seven separate units of 25ns each in the one module or a series connection in 25ns steps up to a maximum of 175ns. The 25ns delay sections are isolated from each other to prevent reflections when only part of the module is connected.

47052 (20ns - 200ns)

It is frequently necessary to have a row of separate delays each of 20ns. This delay module contains 10 separate delays each of 20ns. Space needed on Printed Circuit Boards is much less than if 10 separate delay modules are used, and a single module is easier to handle and solder in production.

The rise times, overshoot, and general pulse quality are compatible with CCIR recommendations.

Since each delay is separated from its neighbour there are no reflection problems from the end of the module if all delay sections are not used.

Fixed

In general it is a little more expensive to manufacture multi pin (programmable or tapped) delay modules. It is also an extra expense to provide the extra holes in Printed Circuit boards.

For this reason the Matthey range of Silver Star Delays contains a large number of "fixed" delay line modules. A variety of impedances is provided from 75Ω to 500Ω.

The range of delays available extends from 5ns to 500ns as shown below.

A special delay line can be designed for your application if a suitable one is not shown in this catalogue.

Technical Data - Pulse P.C.B. Modules

Programmable

Delay Time *ns*	Module No.	Tolerance *ns*	Delay Step *ns*	Impedance *Ω*	Max. Rise Time *ns*	Approx. Weight *gms.*	Size
0·5–9·5	47058		0·5	75	5	4·5	16b
5–35	47022		5	,,	20	4·5	16a
5–155	47001		5	,,	35	11·7	9e
5–235	47064		5	,,	35	25·0	12
10–40	47017		10	,,	8	4·0	17
20–200	47052		20	,,	35	33·0	10b
20–620	47083		20	,,	125	12·0	9d
100–1500	47014		100	,,	180	33·0	10a
Fixed							
25	47011	+2–0		270	25	3·0	19
50	47002	+4–0		75	25	3·0	18
60	47060	±4		,,	30	5·0	15
101·6	47007	±2		,,	35	5·0	15
127	47010/3	±2		,,	12	70·0	8
132	47010/4	±2		,,	12	70·0	8
140	47019	±4		,,	35	10·0	9a
140	47025	±3		270	21	25·0	13
155	47010/1	±3		75	12	70·0	8
160	47010/2	±3		,,	12	70·0	8
203·2	47008	±3		,,	45	10·0	14
406·4	47009	±4		,,	55	19·0	11
435	47024	±5		270	40	19·0	11
Tapped							
175	47061	±4	25ns taps	75	50	12·0	9c
1,000	47003	±30	50ns taps	240	120	33·0	10c

For general data and dimensions see Page 22.

PULSE DELAY LINES

Printed Circuit Board Modules

Tapped

Ten Tapped Series

In this one module size, delay lines from 25ns to 500ns and from 75Ω to 500Ω can be provided.(Photograph 19)

The main feature is that in every "Ten Tapped" module ten tapping points connect to 10% of the total module delay. In this way multiples of 10% can be selected, and if necessary connected in series with other delays to give a vast choice.

It is important to remember when using only a portion of the delay line, that the tapping point, and any other taps so used, must be terminated with an impedance equal to about ten times the design impedance of the module. Also the final section of the delay line should normally be terminated in its design impedance.

75Ω

Engineers usually prefer to work at 500Ω or higher to avoid using the power necessary to drive 75Ω. But, in some circumstances a 75Ω delay is essential and the ten tapped range supplements the "Programmable" modules described on page 17.

270Ω/500Ω

These modules are ideal for use in active circuitry and can be used as supplements to the 500Ω series of fixed delays described on this page.

Fixed

500Ω Series

Each module contains a 500Ω fixed delay from 10ns to 500ns. The data table shows that a variety of rise times is provided. (Photograph 20).

For simplicity of design all modules have the same cross section. The only dimensional change is the length.

A raised pad on the underside prevents moisture being trapped round the lead wires at the module/PCB interface.

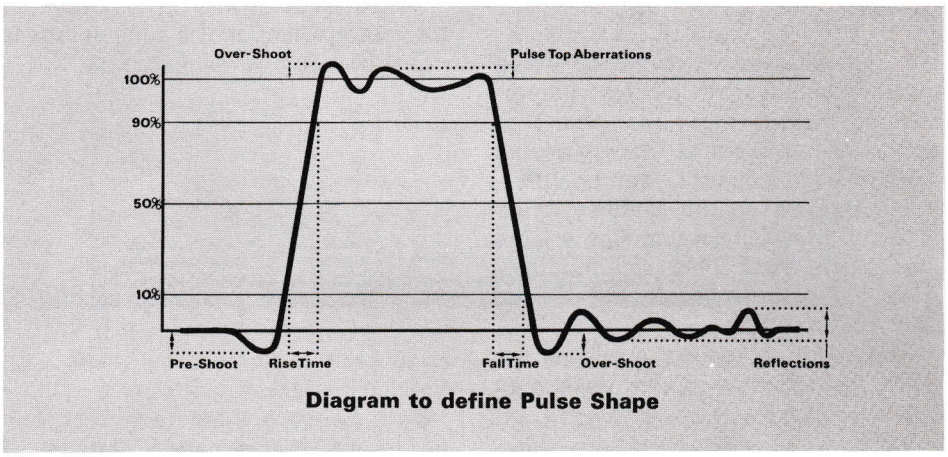
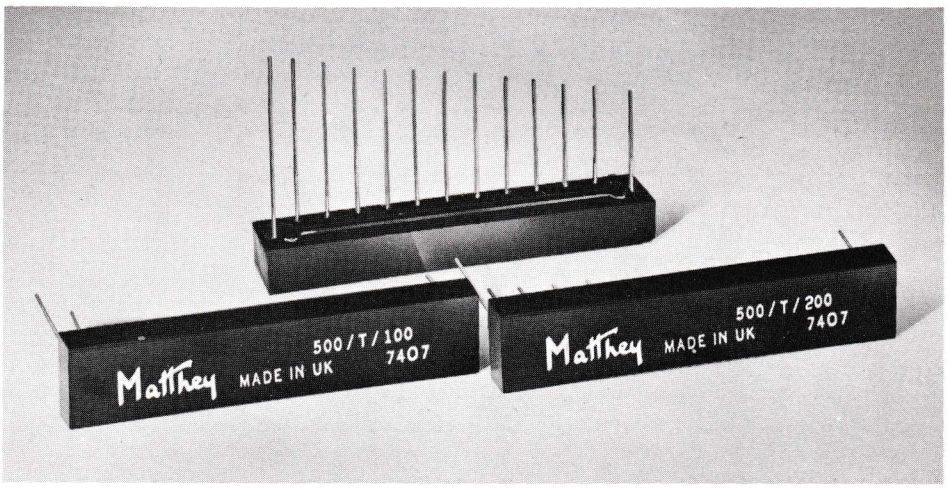
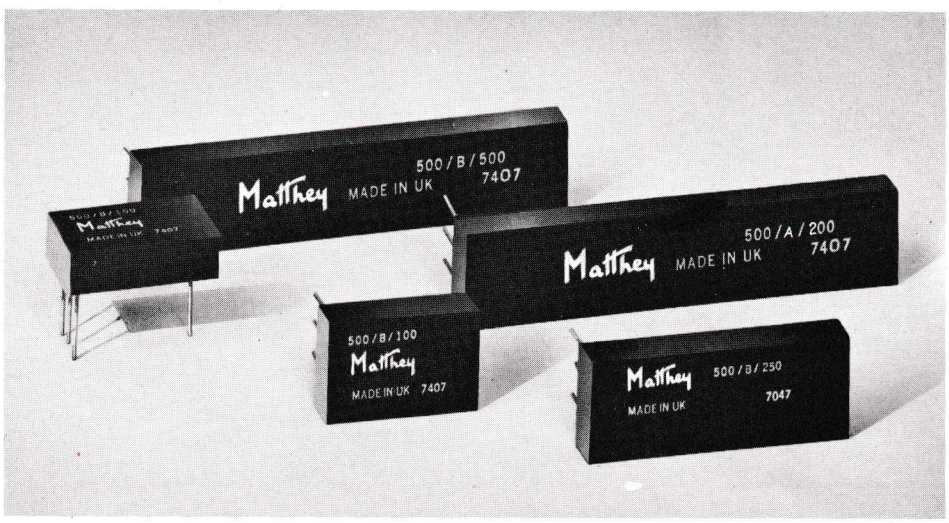


Diagram to define Pulse Shape

19



20



The range shown in the data table is normally available from stock. Special designs can be created to suit your equipment.

500Ω Miniature Delays

This is a small range of building brick modules designed to provide short delays (5, 10 or 20ns) on printed circuit boards using the least possible space. They can be connected in series to provide longer delays if required although we prefer to recommend our larger fixed delay modules when longer delays are required.

Technical Data - Ten Tapped Series

Delay Time *ns*	Module No.	Tolerance *ns*	Delay per Section *ns*	Impedance *Ω*	Max. Rise Time *ns*	Approx. Weight *gms.*	Size
25	75/T/25	±3	2·5±1·5	75	5	11·5	9b
40	75/T/40	±3	4±1·5	,,	8	,,	..
50	75/T/50	±3	5±1·5	,,	10	,,	..
75	75/T/75	±3	7·5±2·5	,,	15	,,	..
100	75/T/100	±2%	10±2·5	,,	20	,,	..
150	75/T/150	±2%	15±2·5	,,	30	,,	..
300	75/T/300	±2%	30±3·0	,,	60	,,	..
50	270/T/50	±3	5±1·5	270	10	,,	..
75	270/T/75	±3	7·5±2·5	,,	15	,,	..
100	270/T/100	±2%	10±2·5	,,	20	,,	..
150	270/T/150	±2%	15±2·5	,,	30	,,	..
200	270/T/200	±2%	20±3·0	,,	40	,,	..
250	270/T/250	±2%	25±3·0	,,	50	,,	..
500	270/T/500	±2%	50±3·0	,,	100	,,	..
50	500/T/50	±3	5±2·5	500	10	,,	..
75	500/T/75	±3	7·5±2·5	,,	15	,,	..
100	500/T/100	±2%	10±2·5	,,	20	,,	..
150	500/T/150	±2%	15±2·5	,,	30	,,	..
200	500/T/200	±2%	20±3·0	,,	40	,,	..
250	500/T/250	±2%	25±3·0	,,	50	,,	..

Technical Data - 500Ω Series

10	500/A/10	+4–0	500	10	3·0	18
40	500/A/40	+4–0	,,	16	5·0	15
100	500/A/100	±2%	,,	21	10·0	14
200	500/A/200	±2%	,,	28	19·0	11
25	500/B/25	+4–0	,,	22	3·0	18
50	500/B/50	+4–0	,,	30	3·0	18
100	500/B/100	±2%	,,	40	5·0	15
250	500/B/250	±2%	,,	54	10·0	14
500	500/B/500	±2%	,,	67	19·0	11
5	500/S/5	+0–1	,,	6	1·5	20
10	500/S/10	+0–2	,,	11	1·5	20
25	500/S/25	+0–4	,,	27	1·5	20

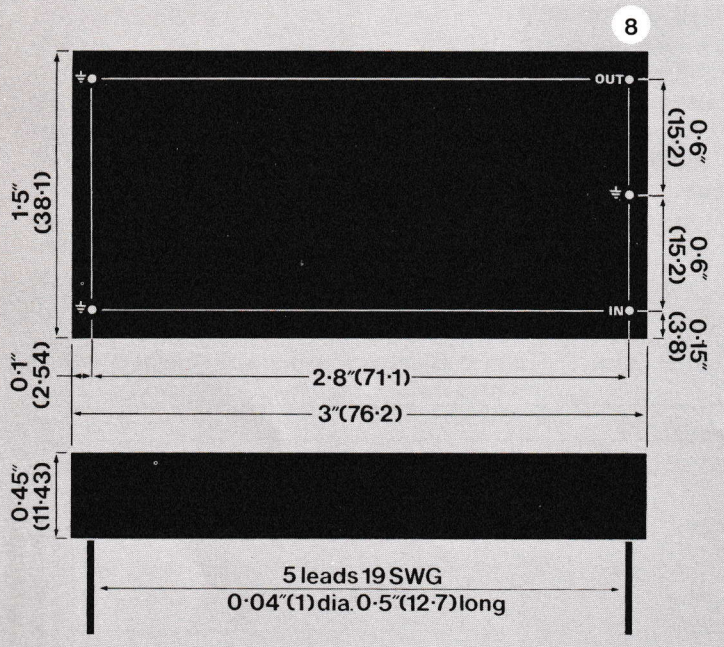
For general data and dimensions see Page 22

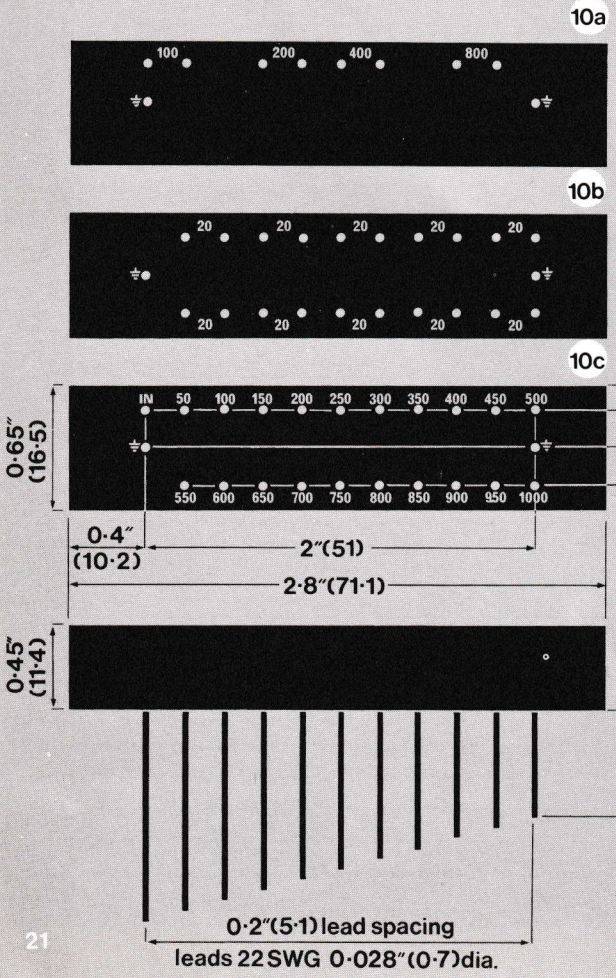
PULSE DELAY LINES

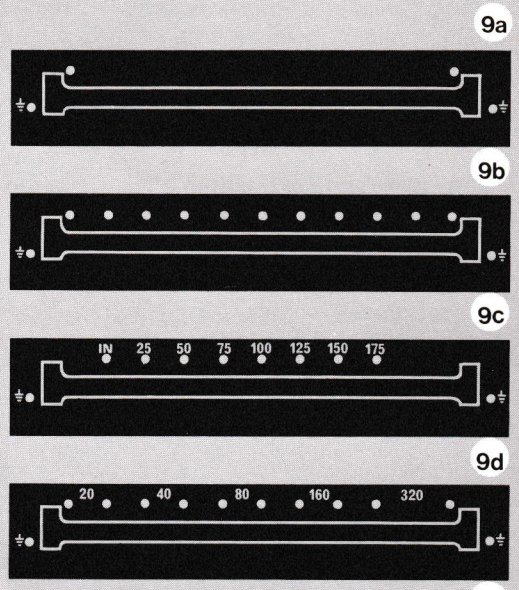
Dimensions & General Data - PCB Modules

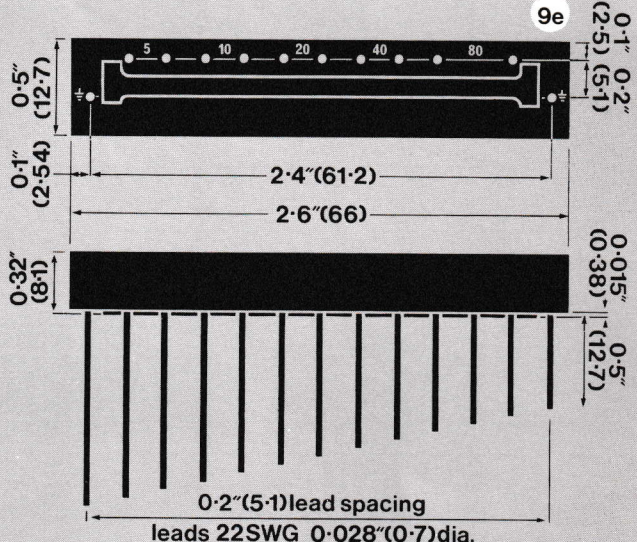
● indicates size number

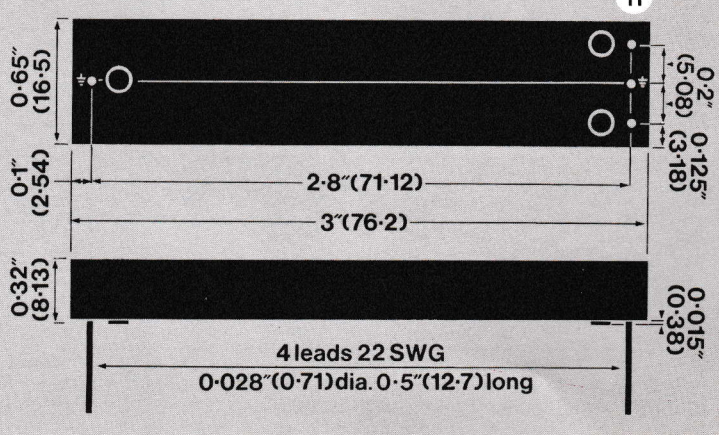
* Small figures within the modules show delay times (ns)
* Lines to pin positions indicate centres
* Millimetre dimensions shown in brackets





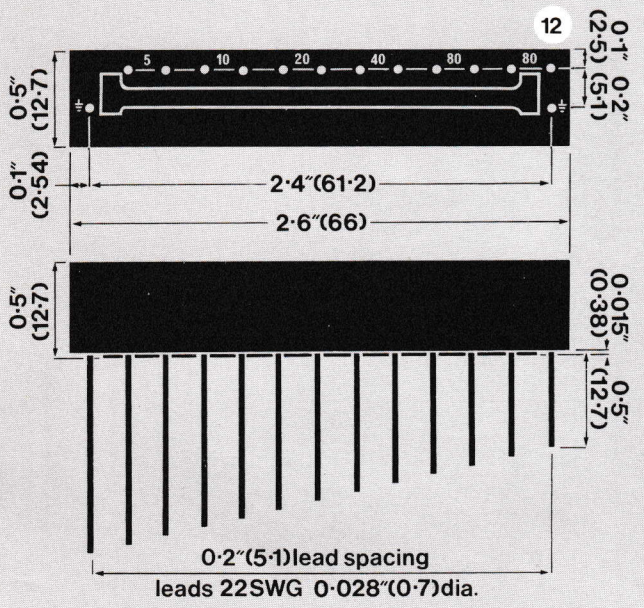


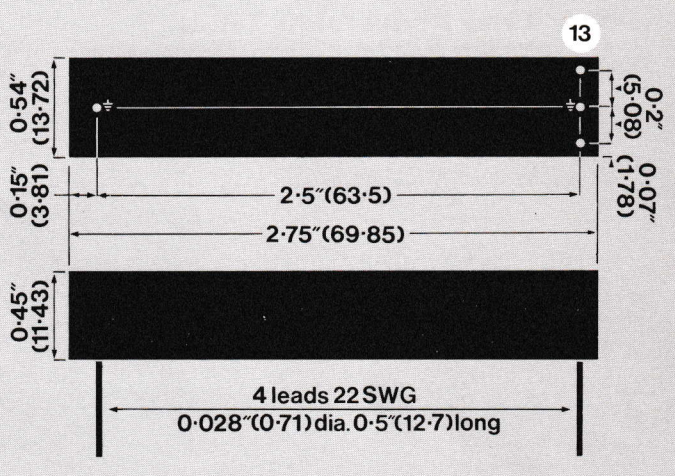


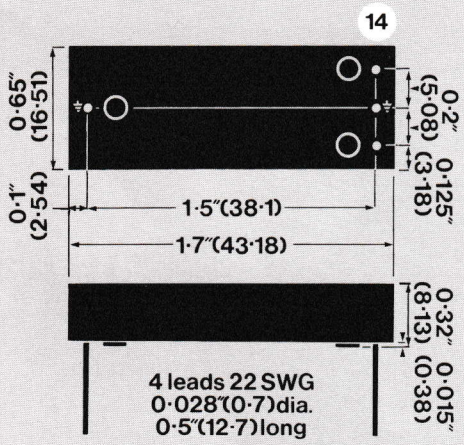


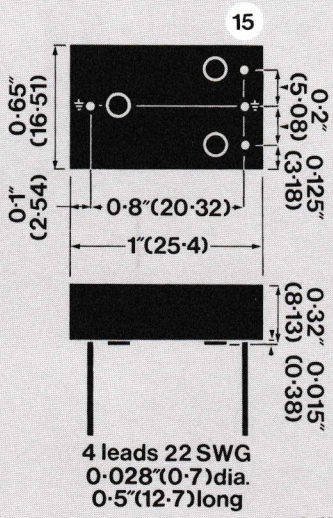
General Data - Pulse P.C.B. Modules

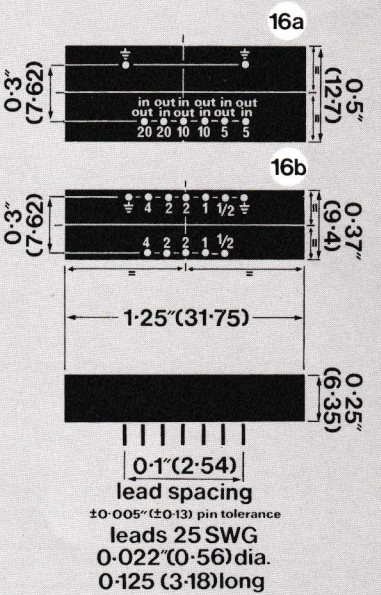
Reflections & Pulse Top Aberrations	Typically within ± 5%
Temperature Coefficient	< +200x10^{-6} per °C Typically 100x10^{-6} per °C
Temperature Range	− 55 °C to + 100 °C
Maximum Input Voltage	5 volts d.c.
Pre-shoot and overshoot	Typically 6%
Overall Pulse Attenuation	Not greater than 2% per 100ns
Finish	Synthetic Resin Encapsulated
Pins	Solder coated phosphor bronze

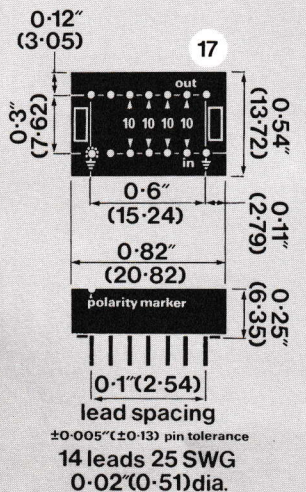


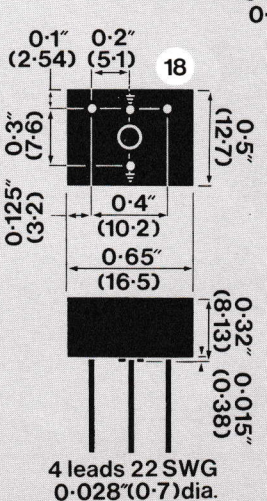


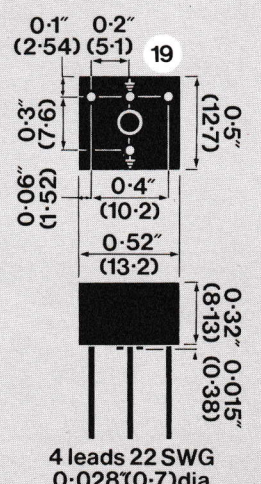


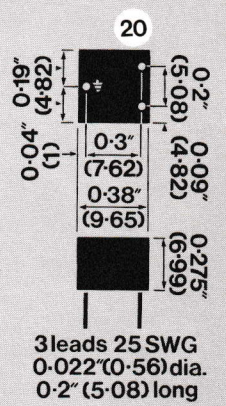












Delay Time Conversion Table

Delay *ns*	Ft.-ins.	Metres	Deg. of phase *PAL*	Deg. of phase *NTSC*
5	3–3	1·00	7·98	6·44
10	6–7	2·00	15·96	12·89
15	9–10	3·00	23·94	19·33
20	13–1	4·00	31·92	25·77
25	16–5	5·00	39·90	32·22
30	19–8	5·99	47·88	38·66
35	22–11	6·99	55·86	45·10
40	26–3	7·99	63·84	51·55
45	29–6	8·99	71·82	57·99
50	32–9	9·99	79·81	64·43
55	36–1	10·99	87·79	70·87
60	39–4	11·99	95·77	77·32
65	42–7	12·99	103·75	83·76
70	45–11	13·99	111·73	90·20
75	49–2	14·99	119·71	96·65
80	52–5	15·98	127·69	103·09
85	55–9	16·98	135·67	109·53
90	59–0	17·98	143·65	115·98
95	62–3	18·98	151·63	122·42
100	65–7	19·98	159·61	128·86
105	68–10	20·98	167·59	135·31
110	72–1	21·98	175·57	141·75
115	75–5	22·98	183·55	148·19
120	78–8	23·98	191·53	154·64
125	81–11	24·98	199·51	161·08
130	85–3	25·97	207·49	167·52
135	88–6	26·97	215·47	173·97
140	91–9	27·97	223·45	180·41
145	95–1	28·97	231·43	186·85
150	98–4	29·97	239·42	193·30
155	101–7	30·97	247·40	199·74
160	104–11	31·97	255·38	206·18
165	108–2	32·97	263·36	212·62
170	111–5	33·97	271·34	219·07
175	114–9	34·97	279·32	225·51
180	118–0	35·96	287·30	231·95
185	121–3	36·96	295·28	238·40
190	124–7	37·96	303·26	244·84
195	127–10	38·96	311·24	251·28
200	131–1	39·96	319·22	257·73
205	134–5	40·96	327·20	264·17
210	137–8	41·96	335·18	270·61
215	140–11	42·96	343·16	277·06
220	144–3	43·96	351·14	283·50
225	147–6	44·96	359·12	289·94
230	150–9	45·95	367·10	296·39
235	154–1	46·95	375·08	302·83
240	157–4	47·95	383·06	309·27
245	160–7	48·95	391·05	315·72
250	163–11	49·95	399·03	322·16
255	167–2	50·95	407·01	328·60
260	170–5	51·95	414·99	335·05
265	173–9	52·95	422·97	341·49
270	177–0	53·95	430·95	347·93
275	180–3	55·95	438·93	354·37
280	183–6	55·94	446·91	360·82
285	186–10	56·94	454·89	367·26
290	190–1	57·94	462·87	373·70
295	193–5	58·94	470·85	380·15
300	196–8	59·94	478·83	386·59
305	199–11	60·94	486·81	393·03
310	203–3	61·94	494·79	399·48
315	206–6	62·94	502·77	405·92
320	209–9	63·94	510·75	412·36
325	213–0	64·94	518·73	418·81
400	262–2	79·92	638·44	515·45
500	327–9	99·90	798·05	644·32
600	393–4	119·88	957·66	773·18
700	458–10	139·86	1117·27	902·05
800	524–5	159·84	1276·88	1030·91
900	590–0	179·82	1436·49	1159·77
1000	655–6	199·80	1596·10	1288·64
1100	721–1	219·78	1755·71	1417·50
1200	786–7	239·76	1915·32	1546·36
1300	852–2	259·74	2074·93	1675·23
1400	917–9	279·72	2234·54	1804·09
1500	983–3	299·70	2394·15	1932·95

N.B. B.I.C.C. co-axial cable T3205 (Velocity Ratio 0·666)

Lignes à retard video

La télédiffusion en couleurs nécessite une synchronisation des signaux très exacte. Souvent ce but est réalisé au moyen d'un câble coaxial supplémentaire de 75Ω de grande longueur. Mais le réglage fin, le prix des compensateurs et des fiches, ainsi que le contrôle du rendement global, voire l'inconvénient qui se produit à installer ces câbles incombrants (souvent sous le plancher), devient de plus en plus coûteux.
Grâce au concours initial prêté par la British Broadcasting Corporation, la Sté. Matthey est en mesure de mettre à la disposition de l'industrie mondiale de télévision la gamme la plus étendue de petites lignes à retard vidéo de 75Ω, contrôlées d'usine et prêtes à être reliées à la route des signaux de télévision en couleurs.
Ces lignes à retard sont actuellement utilisées partout dans le monde dans les studios, les voitures émettrices et les équipements de télévision à circuit fermé. Les ingénieurs-vidéo de Matthey sont toujours disposés à concevoir des modèles particuliers en dehors de ceux décrits dans cette documentation.

Lignes à retard d'impulsions

En vue de retarder les impulsions dans les studios de télévision pour l'enregistrement, pour la diffusion ou la télévision à circuit fermé, il faut des lignes à retard peu coûteux ayant une surmodulation minimale et dont les temps de montée s'accordent avec les préconisations CCIR.
Ce catalogue décrit une gamme étendue de ces dispositifs dont les impédances de 240, 270 ou 500Ω sont compatibles avec le système des circuits actifs. En outre, il existe un grand nombre de retards de 75Ω. Sur la page 15 vous trouverez notre produit le plus récent, soit le coffret retards DO IT YOURSELF.

Video-Laufzeitketten

Beim Farbfernsehen kommt es vor allen Dingen auf eine präzise Synchronisierung der Signale an. Bisher konnte diese häufig durch Zuhilfenahme von zusätzlichen 75Ω Koaxialkabeln erreicht werden. Der Aufwand der damit verbundenen Feinabstimmung, der Entzerrung, der elektrischen Verbindungen, der Verhaltenskontrolle sowie der Unterbringung der nötigen Kabellängen (meistens unter dem Fußboden), wird jedoch immer kostspieliger.
Dank der tatkräftigen Mithilfe der British Broadcasting Corporation steht der internationalen Fernsehindustrie heute bei Matthey die weiteste Auswahl an kleinen 75Ω Video-Laufzeitketten zur Verfügung. Alle Geräte sind werkseits geprüft und können sofort in den Farbsignalweg eingeschaltet werden.
Heute befinden sie sich auf der ganzen Welt im Einsatz in Studios, Übertragungswagen und internen Fernsehanlagen. Die Fernsehingenieure von Matthey begrüßen jederzeit die Möglichkeit, Spezialgeräte zu konstruieren, die über den Umfang dieses Prospektes hinausgehen.

Impuls-Laufzeitketten

Zur Verzögerung von Impulsen in Fernsehstudios, sei es bei der Magnetaufzeichnung, der Übertragung oder bei internen Fernsehanlagen, benötigt man preisgünstige Laufzeitketten mit Anstiegzeiten nach CCIR-Normen und möglichst niedrigem Überschwingverhalten.
In diesem Prospekt wird eine umfangreiche Serie derartiger Laufzeitketten mit Impedanzwerten von 240, 270 und 500Ω beschrieben, welche sämtlich für die Betriebsbedingungen von Nutzkreisen ausgelegt sind. Es steht auch eine reiche Auswahl an 75Ω -Geräten zur Verfügung. Auf Seite 15 finden Sie unsere letzte Neuheit, den DO IT YOURSELF Baukasten.

Lineas de Retardo Video

La emisión televisora en colores exige una sincronización precisa de señales. La realización de tal sincronización ha sido muchas veces posible gracias a la instalación de cortes adicionales de cable coaxial de 75Ω. Sin embargo, los gastos acarreados por la necesidad de un ajuste exacto, de compensadores, de conectadores, de un control general de rendimiento y de encontrar sitio (muchas veces bajo el suelo) para el cable adicional se hacen cada vez más elevados.
Gracias a la ayuda inicial de la British Broadcasting Corporation, la compañía Matthey puede proporcionar a la industria televisora del mundo la gama más extensa de pequeñas líneas de retardo Video de 75Ω todavía puestas a prueba en fábricas y listas para ser introducidas en la ruta de señales de la televisión en colores.
Se utilizan estas líneas de retardo actualmente por todo el mundo en los estudios, en las unidades de emisión exterior y en las instalaciones de television de circuito cerrado. Los ingenieros de la línea de retardo Matthey se preparan para proyectar unidades especiales no incluidas en este catálogo.

Lineas de Retardo de Impulsos

Para retardar los impulsos en los estudios de televisión para la grabación, la emisión y la televisión de circuito cerrado se exigen líneas de retardo de bajo precio cuyos tiempos de subida corresponden a las recomendaciones de la CCIR y cuya sobremodulación es mínima.
Este catálogo describe una gama extensa de dispositivos cuyas impedancias de 240, 270 o 500Ω corresponden al sistema de circuitos activos. Además existen muchos retardos de 75Ω. El producto más reciente es una caja de retardos DO IT YOURSELF (Página 15).

Линии Видеозадержки

Цветное телевизионное вещание нуждается в прецизионном хронировании сигналов, что часто обеспечивается включением дополнительных отрезков коаксиального кабеля 75 омов. Однако, стоимость подстройки, компенсаторов, соединений, проверки рабочих характеристик и прокладки (часто под полом) дополнительных кабелей непрестанно возрастает.

Благодаря первоначальной поддержке со стороны Британской радиовещательной корпорации, фирма Матти в состоянии предложить мировой телевизионной промышленности широкий ассортимент небольших 75-омовых линий видеозадержки, испытанных на заводе и готовых для подключения в сигнальную цепь цветного телевидения.

Эти линии уже широко используются по всему миру в студиях, для внестудийного вещания и в замкнутых телевизионных системах. Техники по видеозадержке фирмы Матти готовы разработать для Вас специальные устройства, не включенные в настоящую брошюру.

Линии Задержки Импульсов

Для задержки импульсов в телевизионных студиях при записи, вещании и для замкнутых телевизионных систем необходимы недорогостоющие линии задержки импульсов со временем нарастания в соответствии с требованиями МККР и с минимальным положительным выбросом.

В настоящей брошюре описан широкий ассортимент этих линий с импедансом в 240, 270 или 500 омов и совместимых с активными схемами. Помимо этого имеется выбор линий задержки в 75 омов. Новейшим нашим продуктом является блок задержки "СВОИМИ РУКАМИ" (стр. 15).

视频延迟线

彩色电视广播的脉冲定时必须高度准确，这个目的往往可以用安装额外长度的75欧姆同轴电缆来达到。但是准确的调整、均衡、连接、全面性能的检验及提供空间(通常是地板下面)以容纳额外电缆愈来愈需要更大的成本。

泰泰公司初期由英国广播公司协助，现在已经能够供应给国际电视界以性能最广泛的经过检验的小型75欧姆视频延迟线，可以直接装入彩色电视信号路线。

这些延迟线目前在世界各国播音室、户外广播单位及有线电视设备中广泛使用。泰泰延迟线工程師随时准备设计不包括在書中的特种延迟线。

脉冲延迟线

錄音、广播及有线电视的脉冲需要成本低的延迟线来延迟，这些延迟线的波升时间必须合乎 CCIR 的规定，而且脉冲过度必须減低到最低限度。

本書介紹具有阻抗 240 欧姆，270 欧姆和 500 欧姆的一系列适应有功线路的延迟线。此外並有大量 75 欧姆的延迟线。最新产品有"自制"延迟箱 (第十五页)。

'ビデオディレーライン'

カラーテレビ放送では、信号の精密なタイミングが要求されます。これは、しばしば75Ω同軸ケーブルを余分に加えることにより調整していますが、正確なトリミングに加えて、等価器、コネクタ、最終特性の検査、設置場所(しばしば床下)等のコストが絶え間なく増加しております。

BBCの援助を仰いで発足したマッセイ社では、現在世界のテレビ産業界に、試験済でカラーテレビ信号系にそのまま挿入できる75Ωビデオディレーラインを供給しております。

弊社のビデオディレーラインは、今や全世界のスタジオ、屋外放送設備、およびCCTVなどに使用されております。弊社の技術陣は、この本に含まれていない特注品の設計も致しております。

'パルスディレーライン'

録画、放送またはCCTVのテレビスタジオにおいて、パルスを遅延させるには、CCIRの推奨する立上り時間と最小のオーバーシュートをもつ低価格のディレーラインが要求されています。

この本には能動回路に適合する240、270、あるいは500Ωのインピーダンスをもつ、広範囲なディレーラインについて記載されております。また75Ωのディレーラインも多数あります。最新の製品としては、DO IT YOURSELFのディレーボックスがあります。
(15ページ)

Matthey Printed Products Limited

A Johnson Matthey Company

William Clowes Street : Burslem : Stoke-on-Trent ST6 3AT : England

Telex 36341: Telegrams + Cables – Matthey Burslem Telex: Telephone – Stoke-on-Trent (0782) 85631

Also ask for data sheets on:

Matthey

Low Pass Video Filters with
phase equalisation

Gaussian Filters
(with rise time to CCIR recommendations)

Chroma Corrector
(puts colour back in its correct place)

Automatic Video Corrector

Viewfinder Mixer

Agent/Distributor

Printed in England by Hill & Ainsworth Ltd., Stoke-on-Trent

AMENDMENTS

Matthey Video and Pulse Delay Line Catalogue 1901

PAGE 4
Revised Technical Data - 3·5 Series

Delay Time *ns*	Model No.	Impedance Ω	Flat Loss at 100KHz *dB*	Size
10—165	3·5/47041	75	<0·65	3·44×3·31 (Front Panel)×3·10ins inc. handle and BNC connectors (87·3×84×78·7mm)
10—325	3·5/360	,,	<1·15	,,
110—265	3·5/47071	,,	<1·15	,,
210—365	3·5/47040	,,	<1·45	,,
310—465	3·5/47050	,,	<1·55	3·44×3·31 (Front Panel)×6·30ins inc. handle and BNC connectors (87·3×84×160mm)
410—565	3·5/47044	,,	<1·65	,,
510—665	3·5/47047	,,	<2·25	,,
610—765	3·5/47048	,,	<2·25	,,
710 865	3·5/47049	,,	<3·05	,,
810—965	3·5/47043	,,	<2·65	,,
910—1065	3·5/47045	,,	<3·25	,,
1210—1365	3·5/47046	,,	<3·85	,,
1810—1965	3·5/47072	,,	<5·85	,,
1910—2065	3·5/47073	,,	<5·95	,,
2710—2865	3·5/47070	,,	<8·45	3·44×3·31 (Front Panel)×7·05ins inc. handle and BNC connectors (87·3×84×179mm)

Finish – Metal Box Anodised Aluminium Front **Operating Temp.** 0°C to 70°C **Connectors** – BNC (Miniquick or Damar and Hagen optional)
Other characteristics correspond to those shown for Video P.C.B. Modules on Page 12

PAGES 9 and 10
Module 47058 has now become Module 47093

PAGE 11
Diagrams 1 and 2b – "In" and "Out" to be reversed.

PAGE 12
General Data – Note that in Switchable Units, UN180, UN360, Series 3·5 and 5·25, the Amplitude/Frequency Response and Return Loss is a function of the delay line combinations used.
Diagram 7 – The overall width on this diagram has been changed to 0·47" (11·9mm).

PAGES 17 and 18
Module 47058 has now become Module 47093
Module 49061 (175 ns tapped) This paragraph has been deleted and now reads . . . . . This delay line provides equipment designers with a useful delay time at 75Ω impedance.

The line is tapped every 25 ns to provide flexibility when used in active circuits. As with all tapped lines, outputs from the taps must be taken at high impedance.

The risetime of 50 ns maximum ensures that it may be used for delaying TV Synchronisation Pulses.

PAGE 20
500Ω Miniature Delays – Delay times are 5, 10 or 25 ns.

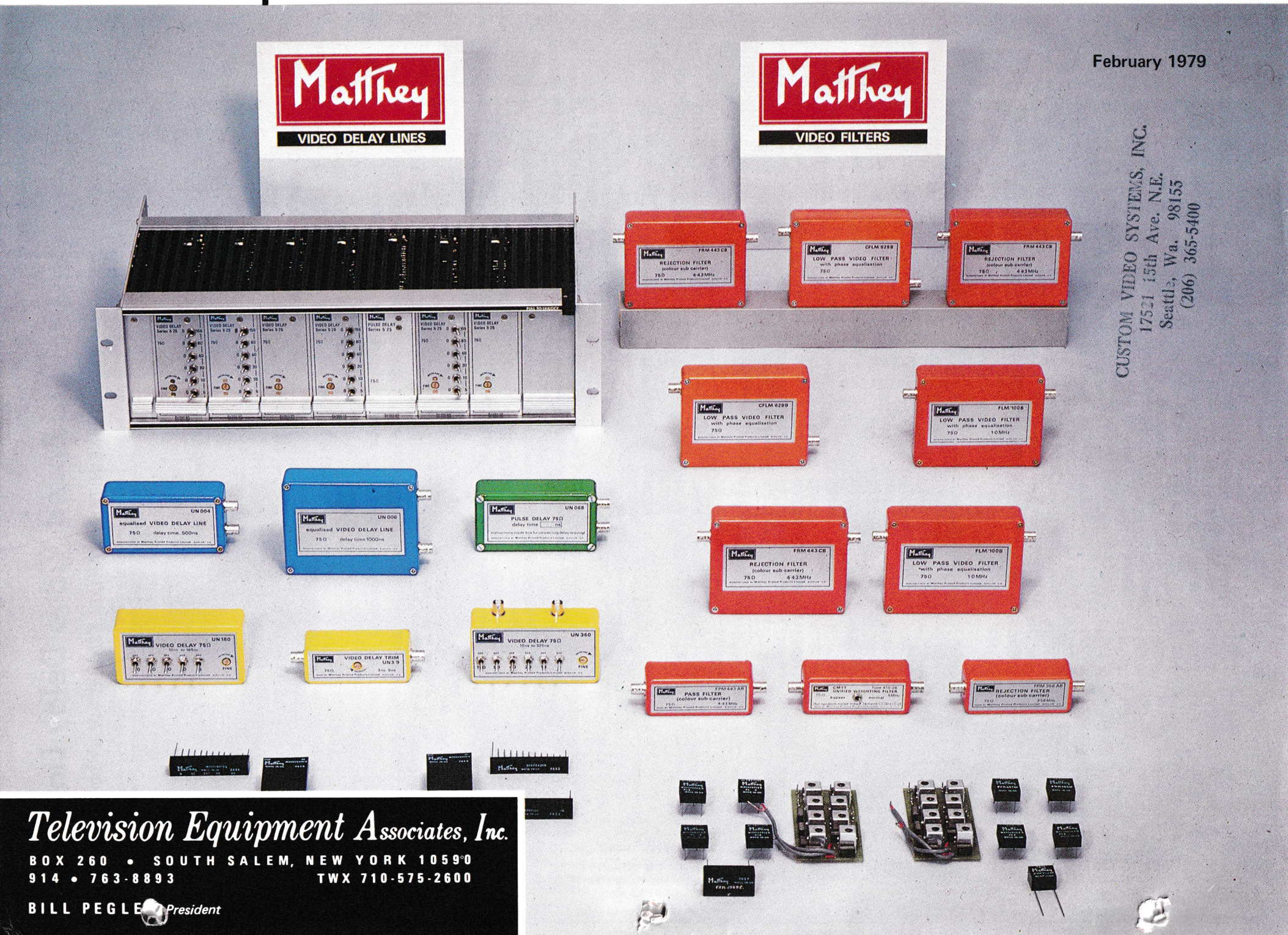
PAGE 21
Diagram 8 – "In" and "Out" to be deleted.

PAGE 22
Diagram 16b – The overall width on this diagram has been changed to 0·47" (11·9mm).

Matthey Video Delay Lines *Price List*

"more stable than cable"

February 1979



CUSTOM VIDEO SYSTEMS, INC.
17521 15th Ave. N.E.
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(206) 365-5400

Television Equipment Associates, Inc.

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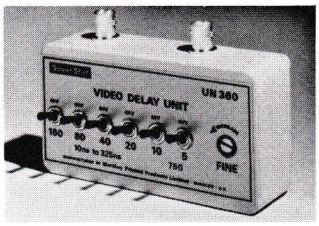
BILL PEGLE *President*



Matthey Boxed Video Delay Lines

INFINITELY VARIABLE VIDEO DELAY BOXES

Two models provide infinitely variable video delay (by means of toggle switches and a ± 4 ns trim) over the following ranges:

Description	*Cable Equivalent*	*Type*	*1-10*	*11-50*
10-165 ns	7-107′	**UN180**	$130.00	$113.00

Performance: Insertion loss/frequency 0.1 dB at low frequency and 0.4 ± 0.1 dB at 4.43 MHz.
Matthey catalog – P. 8

10-325 ns equalized	7-211′	**UN360**	$294.00	$262.00

Performance: Flat loss at 100 KHz at max. delay is 0.9 dB ± 0.2 dB. Return loss is greater than 20 dB up to 5.5 MHz. Amplitude/frequency response – ripple less than 0.4 dB up to 5.5 MHz for any delay.
Matthey Catalog – P. 7, 8

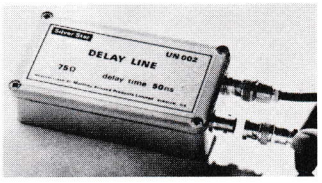
	Type	
Protective Lucite Cover for UN180 and UN360 Matthey Catalog – P. 8	**MLC**	$ 10.00

VIDEO DELAY TRIMMER *(rubber coax)*

An infinitely variable delay range of 3 to 9 ns packaged in a small metal box with BNC connectors – video performance. Recessed screw adjustment permits trimming equivalent to 2-6 feet coax cable. Matthey Catalog – P. 8.

Range	*Cable Equivalent*	*Type*	*1-10*	*11-50*
3-9 ns	2-6′	**UN 3/9**	$ 57.00	$ 51.00

FIXED EQUALIZED VIDEO DELAY BOXES
75Ω – BNC Connectors – 5.5 MHz



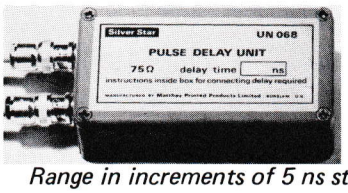
The following equalized lump delay boxes can be cascaded and mixed with UN180 and UN360 to achieve delays to 2000 ns. Amplitude ripple is within 0.2 dB up to 5.5 MHz. A 10 MHz range is also available. Matthey Catalog – P. 6. For other fixed video delays – see back cover of this price list – "Encapsulated Video Delays."

Range	*Cable Equivalent*	*Type*	*1-10*	*11-50*
50 ns	33′	**UN063**	$ 87.00	$ 77.00
100 ns	66′	**UN023**	104.00	92.00
200 ns	133′	**UN005**	123.00	109.00
300 ns	195′	**UN086**	173.00	151.00
500 ns	325′	**UN004**	205.00	181.00
1000 ns	650′	**UN006**	365.00	318.00

NEW – ADJUSTABLE VIDEO DELAY BOXES – 75Ω

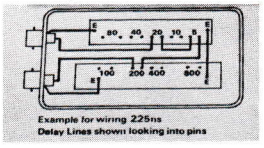
A metal box with BNC connectors containing fixed and segmented video delays in increments of 5 ns with a fine trim of ± 4 ns by screwdriver adjustment on the outside of the box. Instructions inside each box for connection of segmented sections by customer. Except as noted, all units equalized to 5.5 MHz. Data sheet on request.

Adjustable Range	*Cable Equivalent*	*Type*	*1-10*	*11-50*
15-165 ns	10-108′	**UN097/A**	$186.00	$165.00
65-215 ns	43-140′	**UN097/B**	223.00	198.00
115-265 ns	75-173′	**UN097/C**	248.00	220.00
215-365 ns	141-211′	**UN097/D**	295.00	261.00
315-465 ns	207-304′	**UN097/E**	373.00	326.00
415-565 ns	272-369′	**UN097/F**	392.00	341.00
515-665 ns	338-436′	**UN097/G**	415.00	360.00



PULSE and BLANKING DELAY BOX – 75Ω

A metal box with BNC connectors containing pulse delays and instructions for tapping off required delay. Matthey Catalog – P. 15-16.

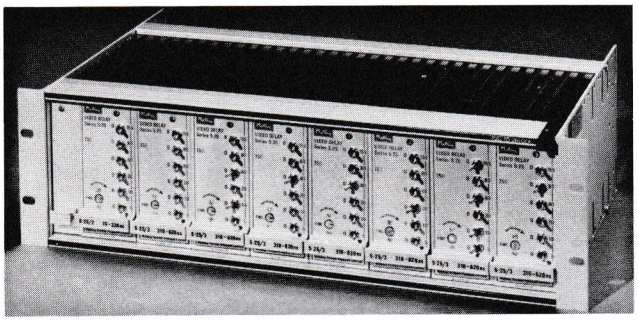


Range in increments of 5 ns steps	*Cable Equivalent*	*Type*	*1-10*	*11-50*
5-155 ns	3½-100	**UN068/A**	$ 69.00	$ 61.00
160-1655 ns	104-1067	**UN068/B**	142.00	140.00
1660-3155 ns	1070-2055	**UN068/C**	301.00	262.00
In increments of 100 ns				
100-1500 ns	66-967	**UN068/1**	116.00	103.00
1600-3000 ns	1032-1935	**UN068/2**	242.00	211.00
3100-4500 ns	2000-2903	**UN068/3**	351.00	305.00

RACK-MOUNTED EQUALIZED VIDEO DELAYS

5.25 SERIES

Matthey Catalog P. 5



5.25 Series Rack Frame $129.00
5.25 Series Blank Panel ..... $ 18.00

The 5.25 series delay line cards are available either with switches (Part No. 5.25/B-) or adjustable (without switches, Part No. 5.25/1A). Both cards have BNC connectors on the back. Up to 8 cards can be accommodated by one rack frame.

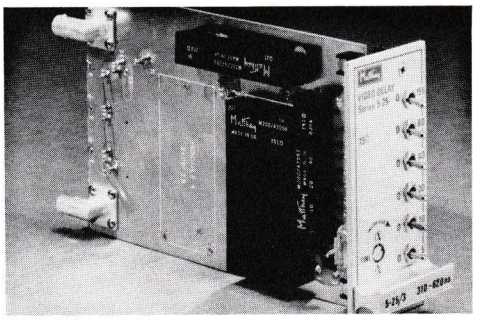
The switched version provides 310 ns.of infinitely variable delay with 6 switches and the ± 4 ns vernier. The version without switches has the ± 4 ns. vernier and is normally supplied with the final 150 ns. segmented range unconnected. You connect this final segmented portion in 5 ns. increments using the ± 4 ns. vernier for fine trim until correct timing is achieved.

With either version, should timing requirements change, Matthey delay line PC modules can be added or subtracted to accommodate any delay requirement from 10 to 2100 ns.

Adjustable Video Delay Cards

5.25/A Series — includes ± 4 ns vernier and Matthey Video Delay modules equalized to 5.5 MHz and padded to 3 dB.

Video Delay Range in nanoseconds	*Type*	*Price*
10 - 165 ns	**5.25/1A**	$ 281.00
115 - 260 ns	**5.25/1B**	309.00
215 - 360 ns	**5.25/1C**	344.00
320 - 460 ns	**5.25/1D**	385.00
410 - 550 ns	**5.25/1E**	413.00
510 - 650 ns	**5.25/1F**	454.00
610 - 745 ns	**5.25/1G**	486.00
715 - 840 ns	**5.25/1H**	519.00
810 - 940 ns	**5.25/1I**	561.00
910 - 1041 ns	**5.25/1J**	595.00
1010 - 1140 ns	**5.25/1K**	629.00
1115 - 1235 ns	**5.25/1L**	666.00
1220 - 1335 ns	**5.25/1M**	691.00
1310 - 1425 ns	**5.25/1N**	719.00
1410 - 1525 ns	**5.25/1P**	760.00
1510 - 1620 ns	**5.25/1Q**	792.00
1610 - 1720 ns	**5.25/1R**	842.00
1710 - 1872 ns	**5.25/1S**	900.00
1820 - 1915 ns	**5.25/1T**	912.00
1910 - 2005 ns	**5.25/1U**	950.00
2000 - 2070 ns	**5.25/1V**	1,016,99
2070 - 2170 ns	**5.25/1W**	1,032.00
2170 - 2250 ns	**5.25/1X**	1,059.00
2110 - 2350 ns	**5.25/1Y**	1,018.00
2210 - 2460 ns	**5.25/1Z**	1,053.00



Switchable Video Delay Cards

5.25/B Series — Six switches and the ±4 ns. vernier provide 310 ns. of infinitely variable delay — equalized to 5.5 MHz and padded to 3 dB.

Video Delay Range	*Type*	*Price*
10 - 320 ns	**5.25/B2**	$ 398.00
310 - 620 ns	**5.25/B3**	529.00
610 - 920 ns	**5.25/B4**	630.00
910 - 1220 ns	**5.25/B5**	702.00
1210 - 1520 ns	**5.25/B6**	835.00
1510 - 1820 ns	**5.25/B7**	877.00
1810 - 2120 ns	**5.25/B8**	1,068.00

Adjustable Pulse Delay Cards

5.25 Series — For delay of pulse and blanking signals using 5.25 PC card — supplied without switches or screwdriver trim. Delay range from 5 ns to 4965 ns. Unless specified on order, units are supplied with minimum delay connected.

Pulse delay range in increments of 5 ns	*in increments of 100 ns*	*Type*	*Price*
5- 155 ns		**5.25/P1**	$ 206.00
160- 310 ns		**5.25/P2**	247.00
315- 465 ns		**5.25/P3**	288.00
	100-1500 ns	**5.25/P4A**	254.00
470-1655 ns		**5.25/P5**	294.00
1660-1810 ns		**5.25/P6**	336.00
1815-1965 ns		**5.25/P7**	376.00
	1600-3000ns	**5.25/P8A**	343.00
1970-3155 ns		**5.25/P9**	383.00
3160-3310 ns		**5.25/P10**	424.00
3115-3465 ns		**5.25/P11**	465.00
	3100-4500ns	**5.25/P12A**	431.00
3470-4655 ns		**5.25/P13**	472.00
4660-4810 ns		**5.25/P14**	513.00
4815-4965 ns		**5.25/P15**	554.00

Note: A small delay module can be fitted to order giving fine trim between 0.5 to 15.5 ns (in 05. ns steps). Add "F" to type number (example 5.25/P1F) and add $61.00 to above prices.

MATTHEY VIDEO EQUIPMENT

See Appropriate Data Sheets

Matthey TV Line Selector 2506 ..... $ 660.00
Matthey Chroma Corrector NTSC:
Standard Model Gain and Delay 3,125.00
Matthey Chroma Corrector NTSC:
With Remote Calibration Knobs and Graph .. 3,350.00
Matthey Chroma Corrector NTSC:
Model with Delay Only — No Gain 2,450.00
Matthey Chroma Corrector NTSC:
Model with 2 Delay Units — No Gain 3,260.00
Matthey Automatic Video Equalizer
NTSC Model 2504 ..... 10,800.00

ENCAPSULATED VIDEO DELAYS FOR PC BOARD MOUNTING – 75Ω

A separate price list covers the entire Matthey range of encapsulated delays for video and pulse with impedances of 75 - 270 and 500 ohm.

See Matthey Catalog – P. 9-12

Description	*Type*	*1-10*	*11-50*	*51 plus*
½ to 9½ ns (in ½ ns steps) equalized for 5.5 MHz	**47093**	$ 44.00	$ 38.00	$ 34.00
½ to 15½ ns (in ½ns steps) equalized for 5.5 MHz	**47094**	57.00	49.00	44.00
5-35 ns (in 5 ns steps) equalized for 5.5 MHz	**47022**	28.00	24.00	21.00
5-155 ns (in 5 ns steps)	**47001**	42.00	37.00	32.00
5-155 ns (in 5 ns steps) equalized for 5.5 MHz	**47051**	114.00	99.00	88.00
5-235 ns (in 5 ns steps) equalized for 5.5 MHz	**47067**	174.00	151.00	134.00
50 ns equalized for 5.5 MHz	**47063**	64.00	56.00	50.00
50 ns.equalized for 10 MHz	**47032**	71.00	61.00	54.00
100 ns equalized for 5.5 MHz	**47023**	84.00	73.00	65.00
100 ns equalized for 10 MHz	**47033**	106.00	92.00	82.00
155 ns equalized for 5.5 MHz	**47085**	110.00	96.00	85.00
160 ns equalized for 5.5 MHz	**47062**	110.00	96.00	85.00
200 ns equalized for 5.5 MHz	**47005**	106.00	92.00	82.00
200 ns equalized for 10 MHz	**47035**	124.00	107.00	95.00
300 ns equalized for 5.5 MHz	**47086**	138.00	112.00	106.00
300 ns equalized for 10 MHz	**47030**	157.00	137.00	121.00
400 ns equalized for 5.5 MHz	**47029**	159.00	138.00	122.00
400 ns equalized for 10 MHz	**47031**	175.00	152.00	135.00
500 ns equalized for 5.5 MHz	**47004**	201.00	174.00	154.00
500 ns equalized for 10 MHz	**47034**	209.00	182.00	161.00
600 ns equalized for 5.5 MHz	**47081**	233.00	202.00	179.00
700 ns equalized for 5.5 MHz	**47095**	257.00	223.00	180.00
800 ns equalized for 5.5 MHz	**47028**	285.00	248.00	219.00
900 ns equalized for 5.5 MHz	**47059**	260.00	235.00	226.00
1000 ns equalized for 5.5 MHz	**47006**	330.00	287.00	254.00
1000 ns equalized for 10 MHz	**47036**	355.00	309.00	273.00
¼ cycle NTSC subcarrier equalized for 5.5 MHz	**47056**	79.00	69.00	61.00
½ cycle NTSC subcarrier equalized for 5.5 MHz	**47057**	106.00	92.00	81.00
360° NTSC & PAL subcarrier equalized for 5.5 MHz	**47066**	259.00	225.00	199.00

Any of the above fixed delay can be supplied in a small metal box with BNC connectors.
Part number on request. Price is cost of delays plus box cost of $34 for 1-10 units and $29 for 11+ units

ENCAPSULATED PULSE DELAYS FOR PC BOARD MOUNTING – 75Ω

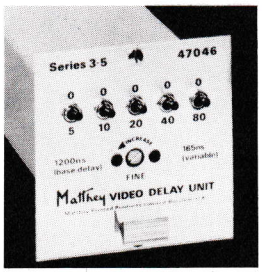
See Matthey Catalog - P. 13-22

Programmable

Delay Time ns	*Type*	*Delay Step ns*	*Impedance Ω*	*1-10*	*11-49*	*50 plus*
10-40	**47017**	10	75	$33.00	$28.00	$25.00
20-200	**47052**	20	75	59.00	52.00	46.00
20-620	**47083**	20	75	60.00	51.00	45.00
100-1500	**47014**	100	75	93.00	81.00	72.00

3.5 SERIES RACK MOUNTED EQUALIZED VIDEO

with 155 ns infinitely variable adjustment.
75Ω – BNC-connectors – rear-mounted
5 units accommodated in 3½" rack panel



This unit consists of a "base delay" (i.e. 50, 100, 200, 300 ns up to 2800 ns.) plus the infinitely variable equalized range 10-165 ns plus the ± 4 ns vernier. The toggle switches and ± 4 ns vernier are panel-mounted. Matthey Catalog – P. 3-4.

Range	*Type*	*1-10*
10-165 ns*	**3.5/47042***	$ 192.00
10-165 ns	**3.5/47041**	242.00
110-265 ns	**3.5/47071**	337.00
210-365 ns	**3.5/47040**	368.00
310-465 ns	**3.5/47050**	399.00
410-565 ns	**3.5/47044**	433.00
510-665 ns	**3.5/47047**	464.00
610-765 ns	**3.5/47048**	492.00
710-865 ns	**3.5/47049**	526.00
810-965 ns	**3.5/47043**	556.00
910-1065 ns	**3.5/47045**	587.00
1210-1365 ns	**3.5/47046**	680.00
1810-1965 ns	**3.5/47072**	953.00
1910-2065 ns	**3.5/47073**	986.00
2010-2165 ns	**3.5/47074**	1,026.00
2710-2865 ns	**3.5/47070**	1,232.00
10-325 ns	**3.5/360**	410.00

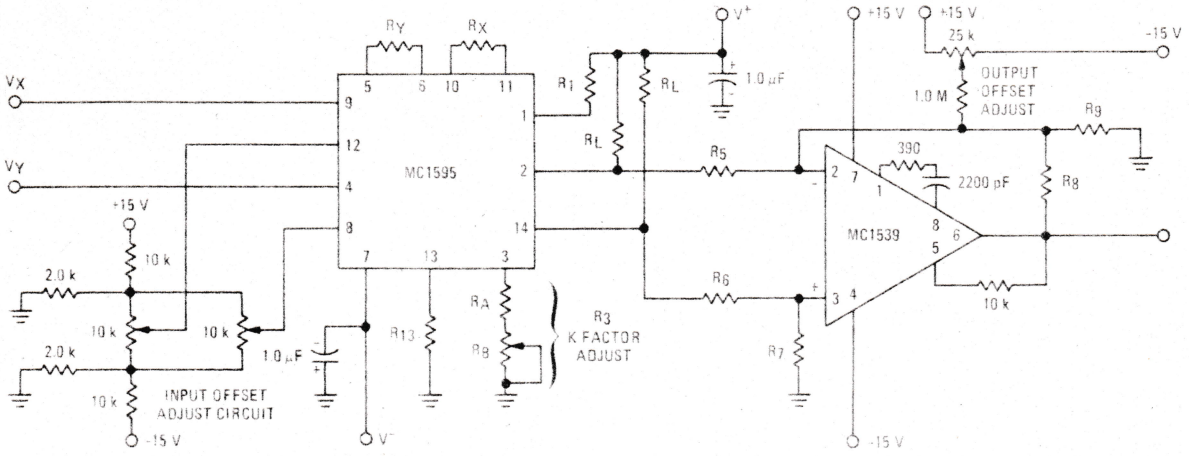
** This delay is not equalized.*

3.5 SERIES ACCESSORIES

	Type	*1-10*
Standard 19" Rack Panel 3½" to accommodate 5	Pa 3/5	$ 55.00
3.5 Series Delay Units Blank inserts for unused openings in panel	PAI 3/5	$ 9.00

TYPICAL APPLICATIONS

FIGURE 10 – MULTIPLY WITH OP-AMP LEVEL SHIFT



RESISTOR	R_1	R_5	R_6	R_7	R_8	R_9	R_{13}	R_A	R_B	R_L	R_X	R_Y
UNIT	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ
TOLERANCE	5%	1%	1%	1%	1%	1%	1%	5%	20%	0.5%	5%	5%
$V^+ = +12$ Vdc, $V^- = -15$ Vdc $10\ V \leq V_X \leq +10\ V$, $10\ V \leq V_Y \leq +10\ V$	9.1	121	100	11	121	15	13.7	12	5.0	1.5	15	15
$V^+ = +15$ Vdc, $V^- = -15$ Vdc $5\ V \leq V_X \leq 5\ V$, $5\ V \leq V_Y \leq 5\ V$	8.0	200	100	100	200	OPEN	13.7	12	5.0	3.4	8.2	8.2

FIGURE 11 – MULTIPLY WITH OP AMP LEVEL SHIFT

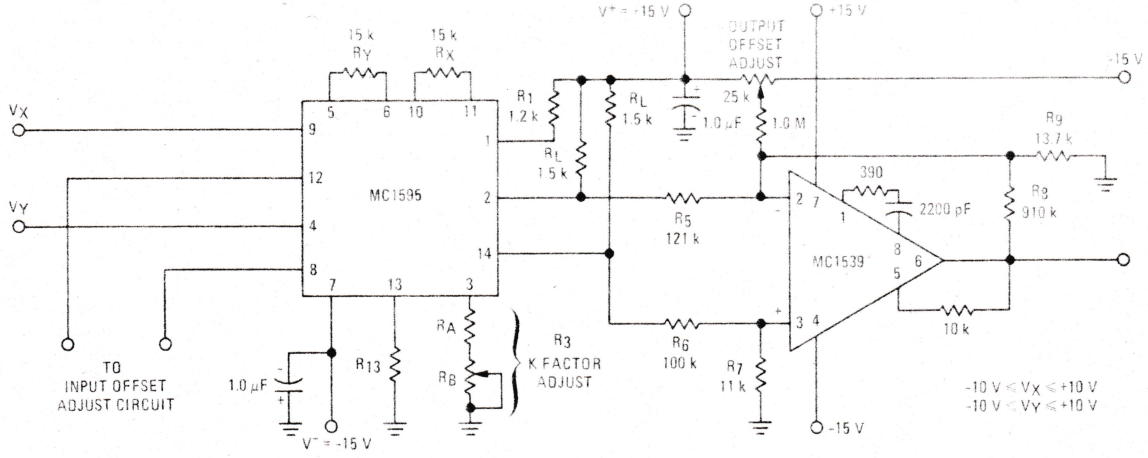
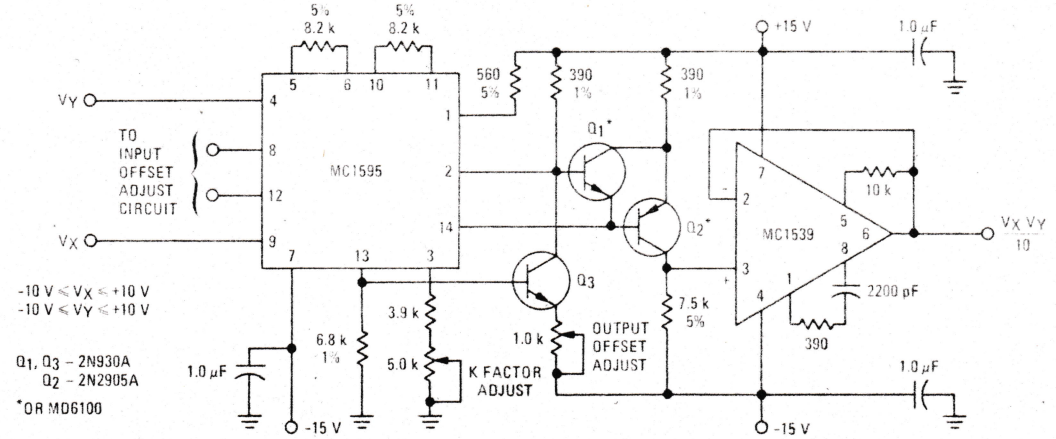


FIGURE 12 – MULTIPLY WITH DISCRETE LEVEL SHIFT



CMOS 8-Bit Buffered Multiplying DAC

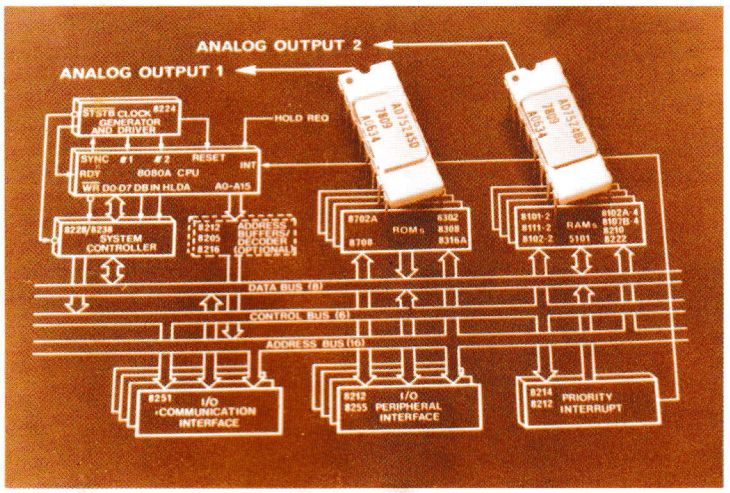
AD7524

FEATURES

- Low Cost
- On-Chip Data Latches
- Full Four-Quadrant Multiplication
- +5 to +15V Operation
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments



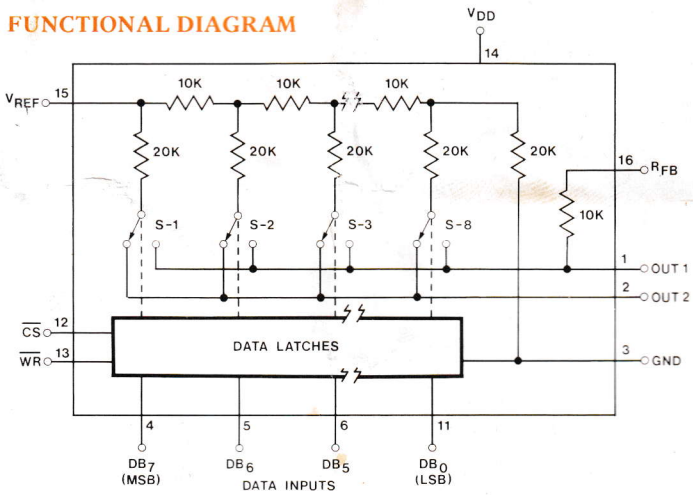
GENERAL DESCRIPTION

The AD7524 is a low-cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8 LSB with power dissipation of only 20 milliwatts.

Featuring operation from +5V to +15V the AD7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

FUNCTIONAL DIAGRAM

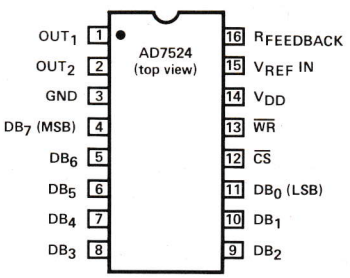


ORDERING INFORMATION

Nonlinearity (V_{DD} = +15V)	Temperature Range and Package		
	Plastic 0 to +70°C	Ceramic -25 to +85°C	Ceramic -55 to +125°C
±1/2 LSB	AD7524JN	AD7524AD[1]	AD7524SD[1]
±1/4 LSB	AD7524KN	AD7524BD[1]	AD7524TD[1]
±1/8 LSB	AD7524LN	AD7524CD[1]	AD7524UD[1]

Note 1: 883B version is available. To order add "/883B" to part number shown. See note 5, page 2.

PIN CONFIGURATION



Route 1 Industrial Park; P.O.Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783
Mid-West 312/894-3300
Texas 214/231-5094

SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

PARAMETER	T_A = 25°C		T_A = Operating Temperature Range		UNITS	TEST CONDITION
	V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
STATIC ACCURACY						
Resolution	8	8	8	8	Bits min	
Nonlinearity						
AD7524JN, AD, SD	±1/2	±1/2	±1/2	±1/2	LSB max	
AD7524KN, BD, TD	±1/2	±1/4	±1/2	±1/4	LSB max	
AD7524LN, CD, UD	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	Guaranteed	Guaranteed	Guaranteed	Guaranteed		
Gain Error[1]	±1.0	±0.5	±1.4	±0.6	% FSR max	
DC Supply Rejection, Gain[2]						
$\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% per % max	ΔV_{DD} = ±10%
Output Leakage Current						
I_{OUT1} (pin 1)	±50	±50	±400	±200	nA max	DB_0 - DB_7 = V_{IH}; $\overline{WR}$, $\overline{CS}$ = V_{IL} V_{REF} = ±10V
I_{OUT2} (pin 2)	±50	±50	±400	±200	nA max	DB_0 - DB_7 = V_{IL}; $\overline{WR}$, $\overline{CS}$ = V_{IL} V_{REF} = ±10V
DYNAMIC ACCURACY						
Output Current Settling Time (to ½LSB)	150[3]	100[3]	200[2]	150[2]	ns max	OUT_1 load = 100Ω; $\overline{WR}$, $\overline{CS}$ = V_{IL} DB_0 - DB_7 = V_{IH} to V_{IL} or V_{IL} to V_{IH}
AC Feedthrough Current[2] @ OUT_1, OUT_2	± ±1/2	±1/2	±1	±1	LSB max	V_{REF} = 100kHz, 20V p-p sine wave; DB_0 - DB_7 = V_{IL} $\overline{WR}$, $\overline{CS}$ = V_{IL}
REFERENCE INPUT						
R_{IN} (pin 15 to GND)[4]	5 20	5 20	5 20	5 20	kΩ min kΩ max	
ANALOG OUTPUTS						
Output Capacitance[2]						
C_{OUT1} (pin 1)	90	90	90	90	pF max	DB_0 - DB_7 = V_{IH}; $\overline{WR}$, $\overline{CS}$ = V_{IL}
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB_0 - DB_7 = V_{IL}; $\overline{WR}$, $\overline{CS}$ = V_{IL}
C_{OUT2} (pin 2)	90	90	90	90	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirements V_{IH}	+3.5	+14.5	+4.0	+14.5	V min	
Input LOW Voltage Requirements V_{IL}	+0.8	+0.5	+0.8	+0.5	V max	
Input Current (per Input) I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance (per Input)[2] C_{IN}	20	20	20	20	pF max	
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[3] t_{CS}	280	180	310	210	ns min	
Chip Select to Write Hold Time[3] t_{CH}	60	50	80	70	ns min	
Write Pulse Width[3] t_{WP}	220	130	240	160	ns min	
Data Setup Time[3] t_{DS}	180	140	200	160	ns min	
Data Hold Time[3] t_{DH}	100	80	120	100	ns min	
POWER SUPPLY						
I_{DD}	500	500	500	500	μA	All Digital Inputs = V_{IL}
	500	500	500	500	μA	All Digital Inputs = V_{IH}

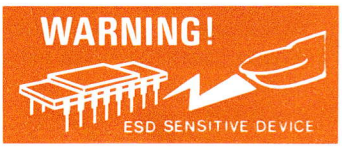
NOTES:
1. Gain error is measured using internal feedback resistor. Ideal Full Scale Range (FSR) = (V_{REF} −1 LSB) as shown in Table 1, page 6.
2. Guaranteed, not tested.
3. AC parameter, sample tested @ 25°C to ensure conformance to specifications.
4. DAC thin film resistor temperature coefficient is approximately −300ppm/°C.
5. 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{IH}, V_{IL}, I_{IN} and I_{DD} at +25°C and +125°C (SD, TD, UD versions) or +25°C and +85°C (AD, BD, CD versions).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

V_{DD} (to GND) . . . . . -0.3V, +17V
V_{RFB} (to GND) . . . . . ±25V
Digital Input Voltage (to GND) . . . . . -0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2)(to GND) . . . . . -0.3V to V_{DD}
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C. 670mW
Derate above +70°C by. . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C. 450mW
Derate above +75°C by. . . . . .6mW/°C
Operating Temperature
Commercial (JN, KN, LN) Grades. . . . . 0°C to +70°C
Industrial (AD, BD, CD) Grades . . . . . -25°C to +85°C
Military (SD, TD, UD) Grades . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 secs). . . . . +300°C

CAUTION:



1. ESD (Electro - Static - Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
2. Do not apply voltages lower than GND or higher than V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V- during power-up or power-down sequencing. To prevent the AD7524 OUT_1 or OUT_2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HSCH 1001 or equivalent) is recommended. The diode should be connected between OUT_1 (OUT_2) and GND as shown in Figures 5 and 6 on page 6.

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a *best straight line* function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle within ½LSB for a given digital input stimulus, i.e. 0 to Full Scale.

GAIN: Ratio of the DAC's full scale operational amplifier output voltage to the reference voltage. "Zero" gain error (for an 8-bit DAC) is defined when $V_{OUT} = -V_{REF}(255/256)$.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT_1 and OUT_2 terminals to GND.

OUTPUT LEAKAGE CURRENT: Current which appears on OUT_1 terminal with all digital inputs LOW or on OUT_2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage (at the amplifier output) of typically 0.2 LSB.

PRICES ($)

MODEL	1 – 24	25 – 99	100 – 499	500 – 999	1000
AD7524JN	7.50	6.00	4.50	3.75	3.00
AD7524KN	10.00	8.00	6.00	5.00	4.00
AD7524LN	12.50	10.00	7.50	6.25	5.00
AD7524AD	12.50	10.00	7.50	6.25	5.00
AD7524BD	15.00	12.00	9.00	7.50	6.00
AD7524CD	17.50	14.00	10.50	8.75	7.00
AD7524SD	31.25	25.00	18.75	15.65	12.50
AD7524TD	37.50	30.00	22.50	18.75	15.00
AD7524UD	43.75	35.00	26.25	21.90	17.50
AD7524AD/883B[5]	19.50	16.00	12.50	10.25	8.00
AD7524BD/883B[5]	22.00	18.00	14.00	11.50	9.00
AD7524CD/883B[5]	24.50	20.00	15.00	12.75	10.00
AD7524SD/883B[5]	38.25	31.00	23.75	19.65	15.50
AD7524TD/883B[5]	44.50	36.00	27.50	22.75	18.00
AD7524UD/883B[5]	50.75	41.00	31.25	25.90	20.50

Note 5: See note 5, page 2.

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE mode:
When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB_0 – DB_7 data bus inputs. In this mode, the AD7524 acts like a non-latched input D/A converter.

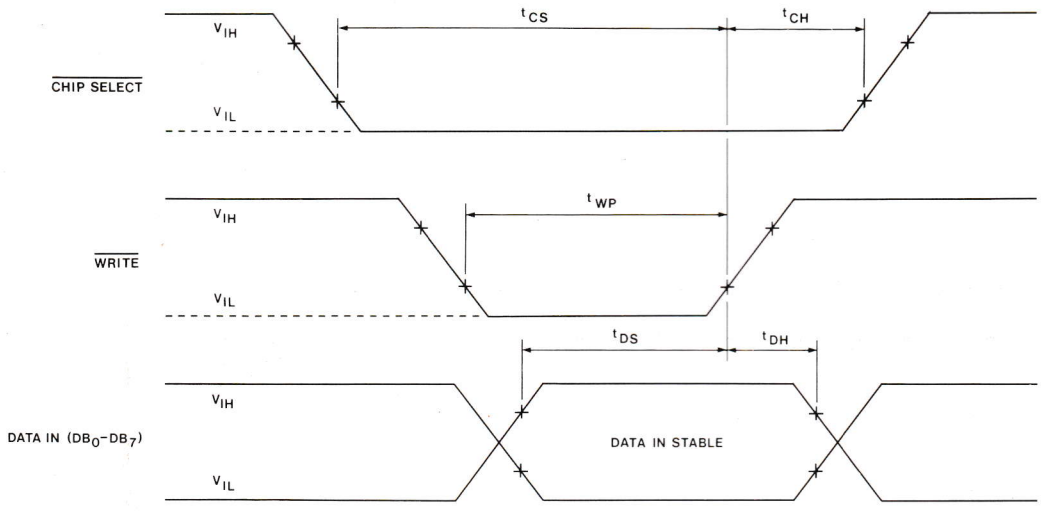
HOLD mode:
When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the AD7524 is in the HOLD mode. In the HOLD mode, the AD7524 analog output holds the value corresponding to the last digital input present at DB_0 – DB_7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB_0 - DB_7) inputs
H	X	HOLD	Data bus (DB_0 - DB_7) is locked out; DAC holds last data present when $\overline{WR}$ assumed HIGH state.
X	H	HOLD	

Note: L = LOW state; H = HIGH state; X = don't care state.

WRITE CYCLE TIMING DIAGRAM



Note: If $\overline{CS}$ and $\overline{WR}$ are exercised simultaneously the t_{DH} specification (as shown in specification table, page 2) must be increased by 60ns.

GENERAL CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT_1 and OUT_2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

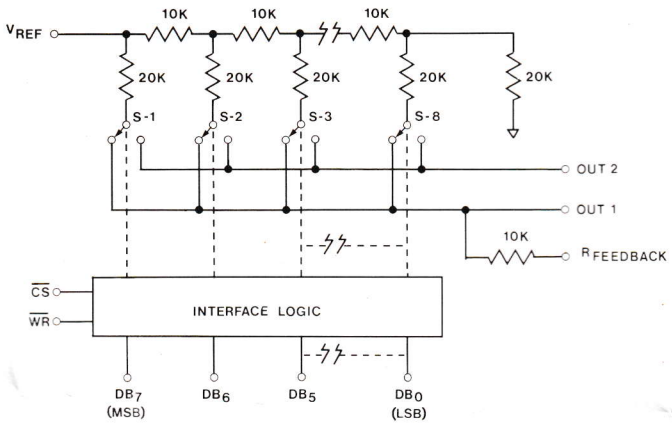


Figure 1. AD7524 Functional Diagram

One of the current switches is shown in Figure 2. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 1 was designed for an "ON" resistance of 20 ohms, switch 2 of 40 ohms, and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

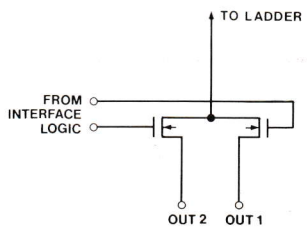


Figure 2. N-Channel Current Steering Switch

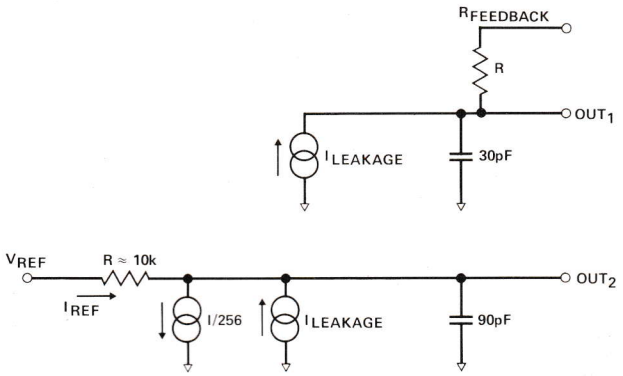


Figure 3. AD7524 DAC Equivalent Circuit - All Digital Inputs LOW

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In figure 3 with all digital inputs LOW, the reference current is switched to OUT_2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/256 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 90pF, as shown on the OUT_2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT_1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT_1, hence the 90pF at that terminal.

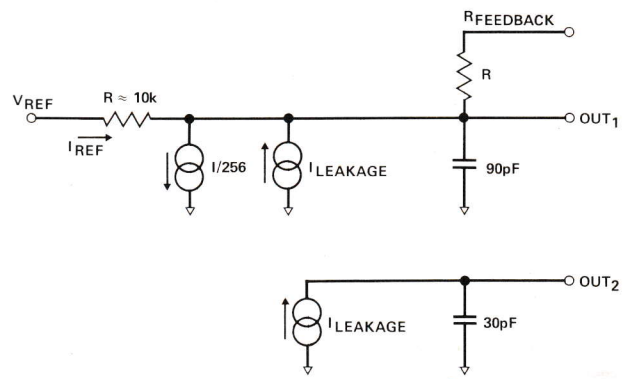
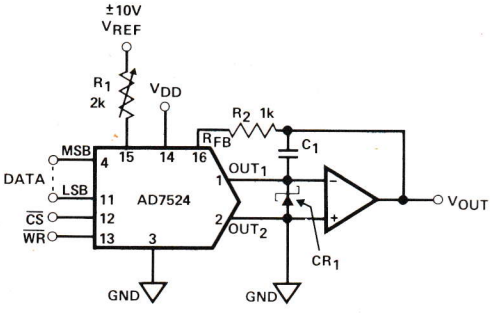


Figure 4. AD7524 DAC Equivalent Circuit - All Digital Inputs HIGH

ANALOG CIRCUIT CONNECTIONS

BASIC OPERATION



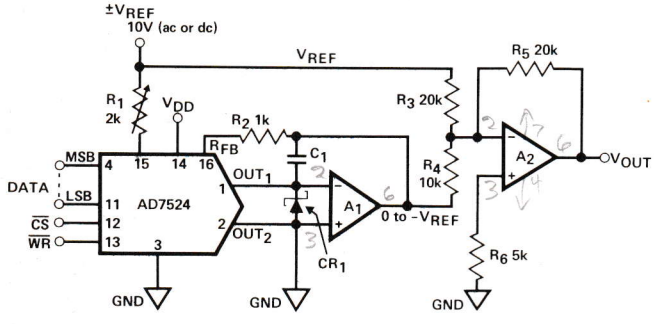
Notes:
1. R1 and R2 used only if gain adjustment is required.
2. CR1 protects AD7524 against negative transients (see "CAUTION" note 3 on page 3).
3. C1 phase compensation (10 - 15pF) is required when using fast amplifiers to prevent ringing or oscillation.

Figure 5. Unipolar Binary Operation (2 - Quadrant Multiplication)

DIGITAL INPUT (MSB … LSB)	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{REF}(\frac{255}{256})$
1 0 0 0 0 0 0 1	$-V_{REF}(\frac{129}{256})$
1 0 0 0 0 0 0 0	$-V_{REF}(\frac{128}{256}) = \frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF}(\frac{127}{256})$
0 0 0 0 0 0 0 1	$-V_{REF}(\frac{1}{256})$
0 0 0 0 0 0 0 0	$-V_{REF}(\frac{0}{256}) = 0$

Note: 1 LSB = $(2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table 1. Unipolar Binary Code Table



Notes:
1. Adjust R1 for VOUT = 0V at code 10000000.
2. C1 phase compensation (10 - 15pF) may be required if A1 is a high speed amplifier.
3. CR1 protects AD7524 against negative transients (see "CAUTION" note 3 on page 3).

Figure 6. Bipolar (4 - Quadrant) Operation

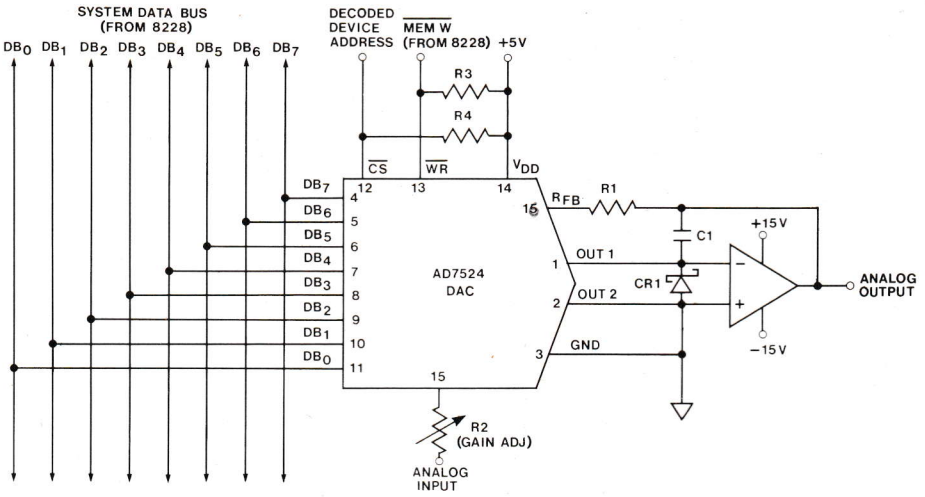
DIGITAL INPUT (MSB … LSB)	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}(\frac{127}{128})$
1 0 0 0 0 0 0 1	$+V_{REF}(\frac{1}{128})$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF}(\frac{1}{128})$
0 0 0 0 0 0 0 1	$-V_{REF}(\frac{127}{128})$
0 0 0 0 0 0 0 0	$-V_{REF}(\frac{128}{128})$

Note: 1 LSB = $(2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

MICROPROCESSOR INTERFACE

AD7524/8080A INTERFACE

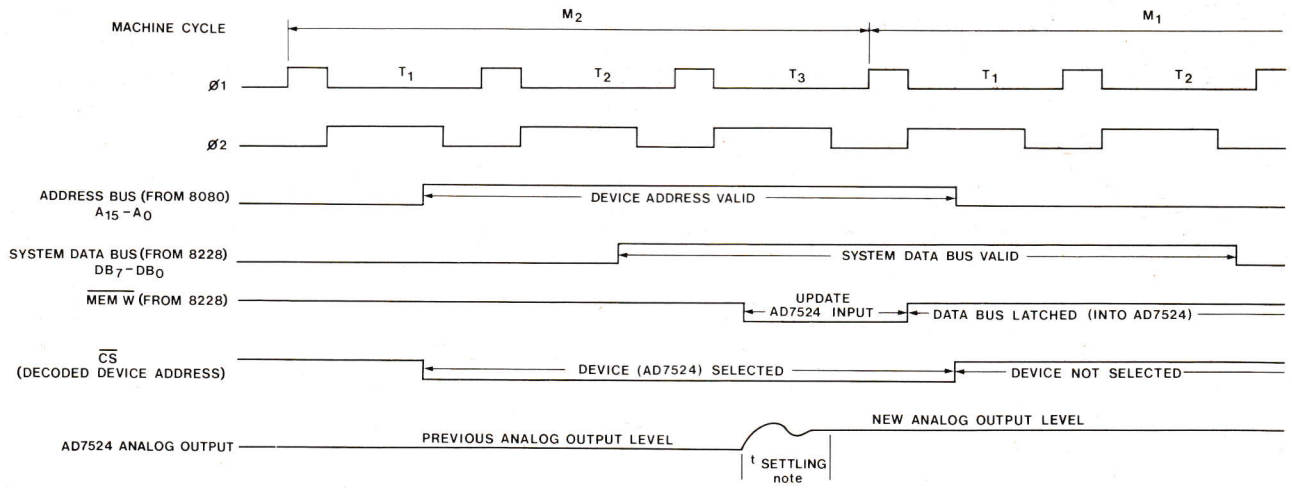


The illustration above shows the AD7524 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080 CPU, 8224 clock generator and 8228 system controller/bus driver. The AD7524 $\overline{WR}$ input is connected to the 8228 $\overline{MEMW}$ output and the DB_0 to DB_7 inputs are connected to the 8228 system data bus outputs. The $\overline{CS}$ input is connected to the system address decoding logic. Note that pullup resistors R_3 and R_4 are required to ensure that the $\overline{CS}$ and $\overline{WR}$ input HIGH states reach 4.0V minimum.

System timing is shown below. Data is loaded into the AD7524 when the $\overline{WR}$ and $\overline{CS}$ inputs are both LOW. The data is latched into the AD7524 when $\overline{WR}$ returns HIGH. AD7524 updating is accomplished by using any of the 8080A memory write instructions (such as MOV M, r).

The AD7524 can also be addressed and loaded as an Isolated Output Device by connecting the AD7524 $\overline{WR}$ input to the 8228 $\overline{I/O\,W}$ terminal (instead of $\overline{MEMW}$).

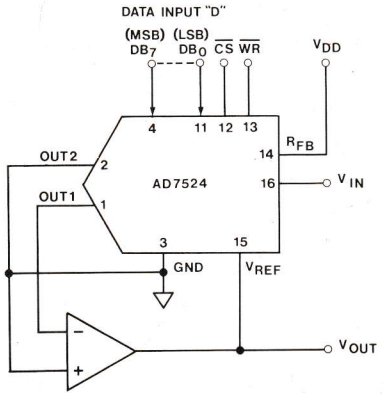
AD7524/8080A INTERFACE TIMING



Note 1. Settling time is dependent primarily upon DAC output amplifier slewing and settling characteristic. Waveform shown is not representative of any specific amplifier.

APPLICATIONS

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$V_{OUT} = \frac{-V_{IN}}{D}$

$A_V = \frac{-V_{OUT}}{V_{IN}} = -\frac{1}{D}$ WHERE: A_V = VOLTAGE GAIN

AND WHERE: $D = \frac{DB_7}{2^1} + \frac{DB_6}{2^2} + \ldots\ldots \frac{DB_0}{2^8}$

DB_N = 1 or 0

EXAMPLES

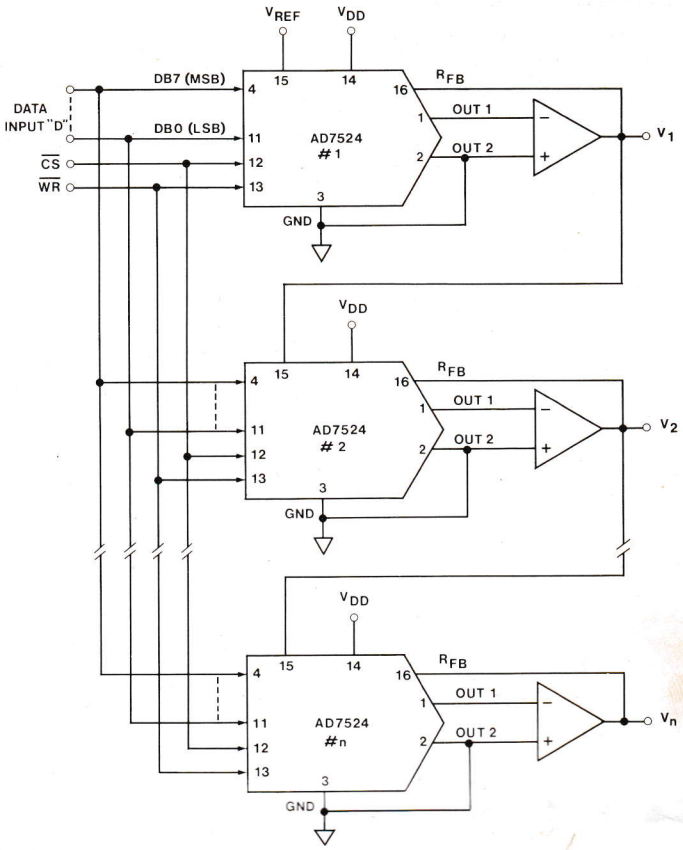
D = 00000000, $A_V = -A_{OL}$ (OP AMP)

D = 00000001, $A_V = -256$

D = 10000000, $A_V = -\frac{256}{128} = -2$

D = 11111111, $A_V = -\frac{256}{255}$

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$

$V_2 = +(V_{REF})(D^2)$

$V_n = -(V_{REF})(D^n)$, n an odd integer

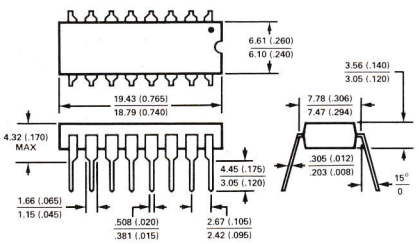
$V_n = +(V_{REF})(D^n)$, n an even integer

WHERE: $D = \frac{DB_7}{2^1} + \frac{DB_6}{2^2} + \cdots \frac{DB_0}{2^8}$

and DB_N = 1 or 0

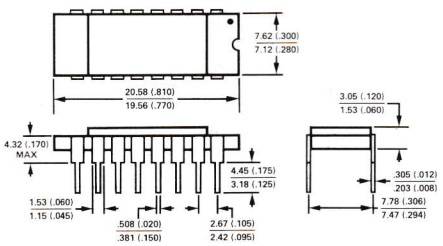
MECHANICAL INFORMATION

16 PIN PLASTIC DIP



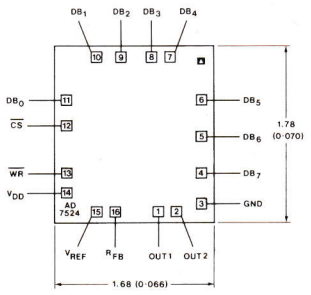
Notes:
1. Lead no. 1 identified by dot or notch.
2. Dimensions in mm (inches).
3. Leads are solder - plated Kovar.

16 PIN CERAMIC DIP



Notes:
1. Lead no. 1 identified by dot or notch.
2. Dimensions in mm (inches).
3. Leads gold - plated (50 microinches min.) Kovar.

BONDING DIAGRAM



Notes:
1. Pad numbers correspond to pin numbers shown in pin configuration (page 1).
2. Dimensions in mm (inches).
3. Pad 3 (GND) should be bonded first to minimize ESD hazards.
4. Pads are 0.102mm x 0.102mm (0.004in. x 0.004in.).

C452a – 8 – 5/79

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Digital Vector Generator

DTM 1716/1717 SERIES

FEATURES

Accurate Sine, Cosine Multiplication
14 Bit Resolution
3 Arc mins Accuracy
0.1% Radius Accuracy
Low Profile (0.4")
Maximum Frequency to Full Accuracy 2.5kHz
Low Feedthrough

APPLICATIONS

Digital to Synchro Conversion
Displays
Axis Rotation
Simulators
Numerical Control
Prediction
Vector Resolution
Spectrum Analysis
Ultra Low Frequency Oscillators

GENERAL DESCRIPTION

The DTM1716 and DTM1717 are computing converters which have a digital angle input in natural binary form and a bipolar analog input $V_i(t)$. There are two analog outputs $V_{01}(t)$ and $V_{02}(t)$, the outputs are related to the inputs by;

$$V_{01}(t) = V_i(t) \sin \phi(t) \qquad V_{02}(t) = V_i(t) \cos \phi(t)$$

where ϕ is the digital angular input. ϕ ranges from 0 to 360°. The analog input has a range of ±10V; the analog output has a range of ±10V.

The digital input has a resolution of 14 bits for the DTM1716 and 12 bits for the DTM1717. The modules are powered from ±15V supply lines.

If the output voltages are regarded as the components of a vector, the radius accuracy is better than 0.1% and the angular inaccuracy is less than 3 arc minutes for the DTM1716.

A block diagram of the DTM1716 is shown in Figure 1.

Particular attention has been paid in the design to achieve high accuracy in the sine and cosine generation so that they may be used separately as accurate functions.

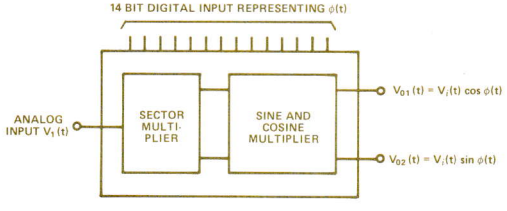
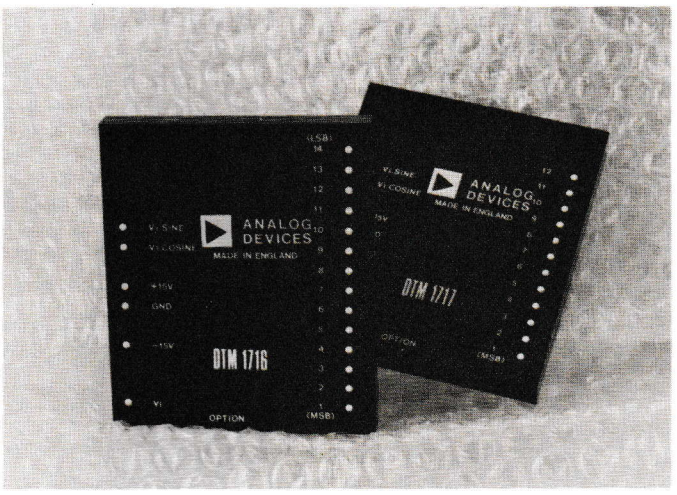


Figure 1. Diagram of DTM1716



Two models are available each with two options as shown below.

DTM1716500 has 14 bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1716600 has 14 bit digital input resolution and a −55°C to +105°C operating temperature.

DTM1717500 has a 12 bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1717600 has a 12 bit digital input resolution and −55°C to +105°C operating temperature range.

OPERATION

The operation of the DTM1716 is straightforward, being powered from ±15V lines relative to the common pin. No damage is caused by either the +15V or −15V being disconnected but they must not be reversed. The analog input is protected against a short circuit to either power line. The output is short circuit proof and can be connected to either power line without damage. The digital inputs are standard TTL levels. The module dimensions and pin out are shown in Figure 2.

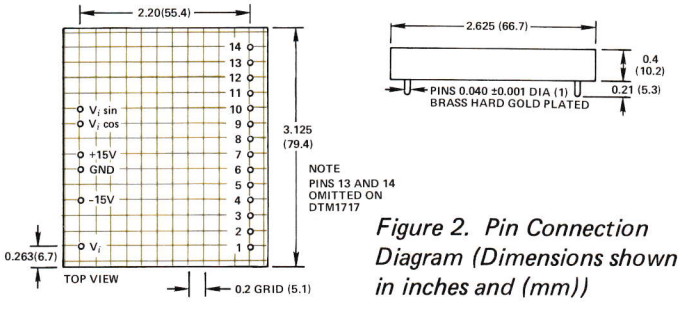


Figure 2. Pin Connection Diagram (Dimensions shown in inches and (mm))

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 **TWX: 710/394-6577**

West Coast	Mid-West	Texas
213/595-1783	312/894-3300	214/231-5094

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODELS	DTM1716	DTM1717
DIGITAL ANGULAR RESOLUTION	14 bits (1 LSB = 1.3 arc-mins)	12 bits (1 LSB = 5.3 arc-mins)
FULL SCALE OUTPUT	±10V	*
SCALING ACCURACY	0.1% FSR	*
FULL SCALE INPUT	±10V	*
SCALE TEMPCO	25ppm/°C of FSR	*
ZERO OFFSET	2.5mV	*
OFFSET DRIFT	50μV/°C	*
AC ACCURACY Analog Step Response (10V Step)	 40μs (to 0.1%)	 *
MAX SLEW RATE	0.5V/μs	*
FULL POWER OUTPUT	8kHz	*
FEEDTHROUGH	<1mV at 400Hz	*
ANALOG INPUT IMPEDANCE	10kΩ	*
ANALOG OUTPUT IMPEDANCE	100mΩ	*
OUTPUT LOAD	2kΩ	*
OUTPUT PROTECTION	Short circuit proof	*
DIGITAL INPUT	14 bit natural parallel binary, 1 TTL Load	12 bits natural parallel binary, 1 TTL Load
RESPONSE TO DIGITAL STEP (90°) (FS Analog Input)	40μs to 0.1% of final value	*
VECTOR ACCURACY[1] Radius Error Angular Error	 0.1% FSR ±3 arc-mins	 * *
POWER SUPPLY REJECTION	80dB	*
POWER SUPPLIES	+15V @ 50mA max -15V @ 40mA max	* *
TEMPERATURE RANGE Operating Storage	0 to +70°C Standard or -55°C to +105°C extended -55°C to +125°C	* * *
DIMENSIONS	3.125 x 2.625 x 0.4" 79.4 x 66.7 x 10.2mm	*
WEIGHT	3 oz (85 grams)	*

NOTES

*Specification same as DTM1716.

[1] See Figure 4.

Specifications subject to change without notice.

APPLICATIONS OF THE DTM1716

Figure 3 shows how the DTM1716 can be used in radars and radar simulators for modulating display sawtooth generators using signals derived from a synchro transmitter on the antenna and a Synchro to Digital converter. The synchro signal representing the antenna angle is converted to a 14 bit natural binary representation by the Synchro to Digital converter SDC1704. The digital angle is applied to the digital input of the DTM1716. A dc voltage is applied to the DTM1716 analog input which controls the radius of the displayed raster. The output voltages are used to provide the X and Y time base currents. The switches across the capacitors are opened on the leading edge of the transmission pulse and closed after a time interval determined by the range.

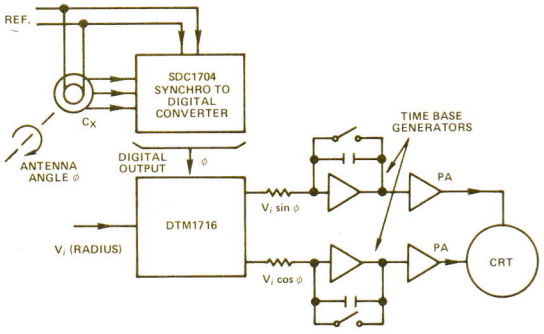


Figure 3. PPI Waveform Generation Using the DTM1716

AXIS ROTATION

Figure 4 shows how two DTM1716's may be used to compute the new two dimensional coordinates of a point relative to a rotated set of axes. The input voltage X_1 and Y_1 are proportional to the coordinates of a point in the XY plane. If a digital angle ϕ is applied to the DTM1716's, the output voltages X_2 and Y_2 correspond to the X and Y coordinates of the point relative to a set of axes rotated through the angle ϕ. The systems can be extended to three dimensions.

The arrangement as shown in Figure 4 may also be used to obtain the new coordinates of a point which is rotated through the angle in the same coordinate set. This scheme provides a low cost, accurate and compact solution to transformation problems.

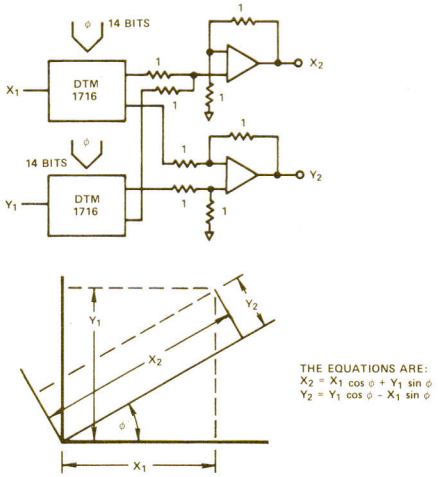


Figure 4. Axis Rotation in Two Dimensions Using the DTM1716

SYNCHRO TO INVARIANT SINE/COSINE

In many engineering applications it is required to obtain voltages proportional to the sine and cosine of an angular movement and to be able to scale the voltages electrically. Figure 5 shows how a Synchro to Digital converter and the DTM1716 may be used for this purpose. The advantage of this scheme is that the coefficients of sine and cosine are electrically scalable by means of the bipolar voltage V_i, saving memory space, multipliers, power and space.

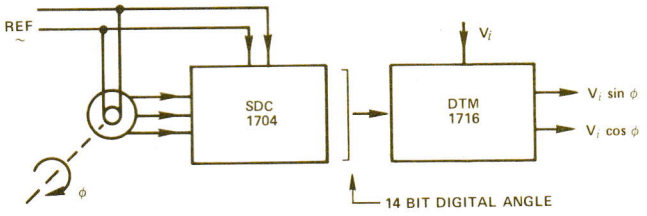


Figure 5. Synchro to Invariant Sine/Cosine Using the SDC1704 and DTM1716

POWER SPECTRUM ANALYSIS

Figure 6 shows a less usual application of the DTM1716 in the spectrum analysis of low frequency signals. This has the advantage of providing almost infinite resolution at extremely low relative cost.

A simple method of obtaining the power in the frequency interval $f \pm \Delta f$ is shown in Figure 6.

The input waveform from which the power spectrum is required is g(t). Multiplication of this waveform by Sin $2\pi ft$ causes the energy in the waveform between $f - \Delta f$ and $f + \Delta f$ to be shifted to lie between $-\Delta f$ and $f + \Delta f$. The low pass filter passes this voltage waveform to the square law devices to produce an output proportional to the power. Two channels, sine and cosine, are used for the case where g(t) may contain a periodic component. If for example there is a line in the power spectrum, without the use of the two channels the output at that frequency would depend upon its phase. The use of both sine and cosine multiplication avoids this problem.

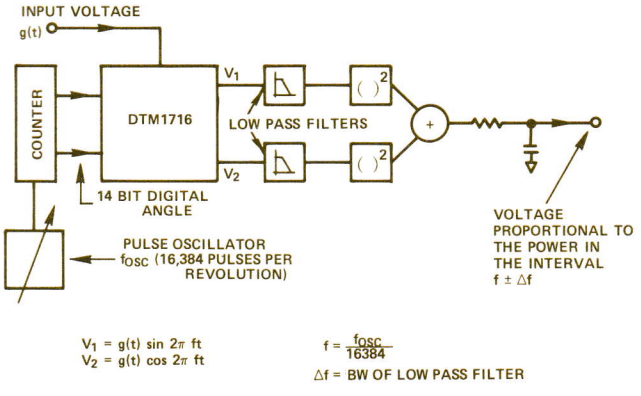


Figure 6. The Use of the DTM1716 to Obtain the Power Frequency Spectrum of g(t)

PHASE MODULATION

The DTM1717 can be used for low frequency phase modulation of subcarriers. Figure 7 shows the method which uses two DTM1717's and an ADC. Frequency modulation can be obtained if the amplitude of the signal is made to be inversely proportional to its frequency. This can be accomplished by inserting an integrator in series with the modulation input. Similar techniques can be used for very low frequency synthesis.

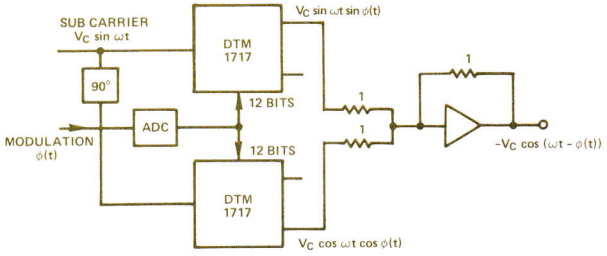


Figure 7. Phase Modulation Using 2 DTM1717's

ORDERING INFORMATION

There are only two options for each of the DTM1716 and DTM1717. They are the commercial or extended temperature ranges. The appropriate designations are as follows:

DTM1716500 (14 bits) 0 to +70°C
DTM1716600 (14 bits) -55°C to +105°C
DTM1717500 (12 bits) 0 to +70°C
DTM1717600 (12 bits) -55°C to +105°C

OTHER PRODUCTS

Many modules concerned with the conversion of synchro data are manufactured by us, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

SYNCHRO TO DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4″) converter with a 12 bit natural binary output. Its overall accuracy is ±8.5 arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz.

The SDC1702 is similar to the new SDC1700 but has a 10 bit natural binary output and an overall accuracy of +22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14 bit natural binary output and an overall accuracy of ±2.0 arc-minutes ±1LSB.

The SBCD1752/1753/1756 and 1757 are Synchro to Digital converters based on the SDC1700 which give an output in BCD format.

DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 14 bits are available as well as the DSC1710 which is a one card, 1 channel, two speed DSC system containing its own 20VA power amplifiers.

TWO SPEED PROCESSORS

The TSL1612 combines the digital outputs of the two Synchro to Digital converters in a two speed system in order to produce a single digital word representing the input angle. It is available for any ratio between 2:1 and 36:1.

C463–18–5/78

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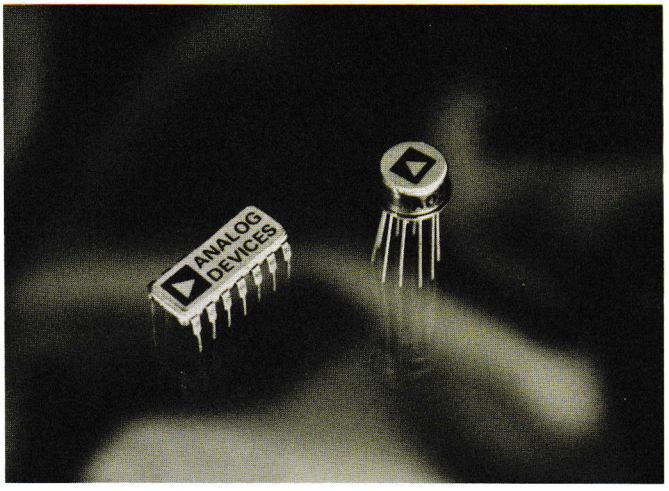
ANALOG DEVICES

Low Cost IC Multiplier,Divider,Squarer,Square Rooter

AD533

FEATURES

- Simplicity of Operation: Only Four External Adjustments
- Max 4-Quadrant Error Below 0.5% (AD533L)
- Low Temperature Drift: 0.01%/°C (AD533L)
- Multiplies, Divides, Squares, Square Roots



PRODUCT DESCRIPTION

The Analog Devices AD533 is a low cost integrated circuit multiplier comprised of a transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. Specified accuracy is easily achieved by the straight-forward adjustment of feedthrough, output zero, and gain trim pots. The AD533 multiplies in four quadrants with a transfer function of XY/10, divides in two quadrants with a 10Z/X transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10Z}$. Several levels of accuracy are provided: the AD533J, AD533K, and AD533L, for 0 to +70°C operation, are specified for maximum multiplying errors of 2%, 1%, and 0.5% respectively at +25°C. The AD533S, for operation from −55 to +125°C, is guaranteed for a maximum 1% multiplying error at +25°C. The maximum error specification is a true measure of overall accuracy since it includes the effects of offset voltage, feedthrough, scale factor, and nonlinearity in all four quadrants.

The low drift design of the AD533 insures that high accuracy is maintained with variations in temperature. The op amp output provides ±10 volts at 5mA, and is fully protected against short circuits to ground or either supply voltage: all inputs are fully protected against over-voltage transients with internal series resistors. The devices provide excellent ac performance, with typical small signal bandwidth of 1.0MHz, full power bandwidth of 750kHz, and slew rate of 45V/μsec.

The low cost and simplicity of operation of the AD533 make it especially well suited for use in such widespread applications as modulation and demodulation, automatic gain control and phase detection. Other applications include frequency discrimination, RMS computation, peak detection, voltage controlled oscillators and filters, function generation, and power measurements.

All models are available in the hermetically-sealed TO-100 metal can and TO-116 ceramic DIL packages.

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS (typical @ +25°C, externally trimmed and V_S = ±15VDC unless otherwise specified)

PARAMETER	CONDITIONS	AD533J	AD533K	AD533L	AD533S
ABSOLUTE MAX RATINGS					
Internal Power Dissipation		500mW	*	*	*
Input Voltage (Note 1)					
X_{in}, Y_{in}, Z_{in}, X_o, Y_o, Z_o		$\pm V_S$	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	−55 to +125°C
Storage Temp Range		−65 to +150°C	*	*	*
Output Short Circuit	To Ground	Indefinite	*	*	*
MULTIPLIER SPECIFICATIONS					
Transfer Function		XY/10	*	*	*
	Untrimmed	XY/6 max [XY/10 min]	*	*	*
Total Error (of full scale)		±2.0% max	±1.0% max	±0.5% max	±1.0% max
	T_A = min to max	±3.0%	±2.0%	±1.0%	±1.5%
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.01%/°C
Nonlinearity					
X Input	$V_X = V_O$ = 20V(p-p)	±0.8%	±0.5%	**	**
Y Input	$V_Y = V_O$ = 20V(p-p)	±0.3%	±0.2%	**	**
Feedthrough					
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	150mV(p-p) max	200mV(p-p) max	50mV(p-p) max	100mV (p-p) max
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	200mV(p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
DIVIDER SPECIFICATIONS					
Transfer Function		10Z/X	*	*	*
	Untrimmed	10Z/X max [6Z/X min]	*	*	*
Total Error (of full scale)	V_X= −10VDC, V_Z= ±10VDC	±1.0%	±0.5%	±0.2%	±0.5%
	V_X= −1VDC, V_Z= ±10VDC	±3.0%	±2.0%	±1.5%	±2.0%
SQUARER SPECIFICATIONS					
Transfer Function		$X^2/10$	*	*	*
	Untrimmed	$X^2/6$ max [$X^2/10$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
SQUARE ROOTER SPECIFICATIONS					
Transfer Function		$-\sqrt{10Z}$	*	*	*
	Untrimmed	$-\sqrt{10Z}$ max [$-\sqrt{6Z}$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
INPUT SPECIFICATIONS					
Input Resistance					
X Input		10MΩ	*	*	*
Y Input		6MΩ	*	*	*
Z Input		36kΩ	*	*	*
Input Bias Current					
X, Y Inputs		3μA	7.5μA max	5μA max	7.5μA max
Z Input		±25μA	*	*	*
X, Y Inputs	T_A = min to max	12μA	10μA	7μA	7μA
Z Input	T_A = min to max	±35μA	*	*	*
Input Voltage	T_A = min to max				
V_X, V_Y, V_Z	For Rated Accuracy	±10V	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μsec	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Sm Sig 1% Vector Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μsec to 2%	*	*	*
Overload Recovery		2μsec to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance		100Ω	*	*	*
Output Voltage Swing	T_A = min to max				
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		Trimmable To Zero	*	*	*
vs. Temperature	T_A = min to max	0.7mV/°C	*	*	*
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	Rated Performance	±15V	*	*	*
	Operating	±15V to ±18V	±10V to ±18V	±10V to ±18V	±10V to ±22V
Supply Current	Quiescent	±6mA max	*	*	*
Power Supply Variation	*Includes* Effects of Recommended Null Pots				
Multiplier Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor		±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

Note 1: Max input voltage is zero when supplies are turned off.

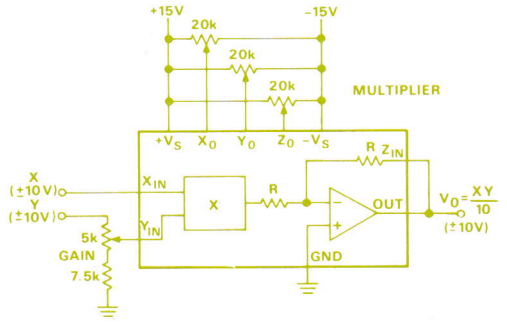
*Specifications same as AD533J

**Specifications same as AD533K

Specifications subject to change without notice.

MULTIPLIER

Multiplier operation is accomplished by closing the loop around the internal op amp with the Z input connected to the output. The X_O null pot balances the X input channel to minimize Y feedthrough and similarly the Y_O pot minimizes the X feedthrough. The Z_O pot nulls the output op amp offset voltage and the gain pot sets the full scale output level.



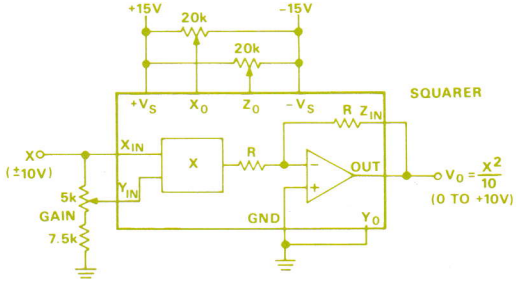
TRIM PROCEDURES

1. With X = Y = 0 volts, adjust Z_O for 0VDC output.
2. With Y = 20 volts p-p (at f = 50Hz) and X = 0V, adjust X_O for minimum ac output.
3. With X = 20 volts p-p (at f = 50Hz) and Y = 0V, adjust Y_O for minimum ac output.
4. Readjust Z_O for 0VDC output.
5. With X = +10VDC and Y = 20 volts p-p (at f = 50Hz), adjust gain for output = Y_{in}.

NOTE: For best accuracy over limited voltage ranges (e.g., ±5V), gain and feedthrough adjustments should be optimized with the inputs in the desired range, as linearity is considerably better over smaller ranges of input.

SQUARER

Squarer operation is a special case of multiplier operation where the X and Y inputs are connected together and two quadrant operation results since the output is always positive. When the X and Y inputs are connected together, a composite offset results which is the algebraic sum of the individual offsets which can be nulled using the X_O pot alone.

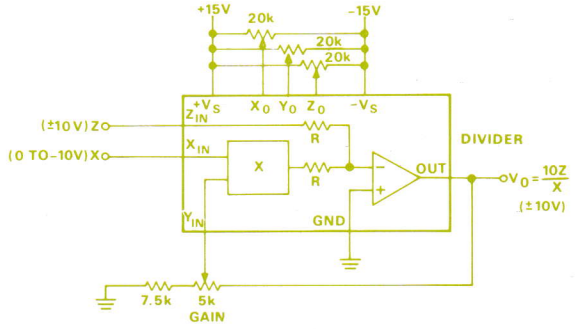


TRIM PROCEDURES

1. With X = 0 volts, adjust Z_O for 0VDC output.
2. With X = +10VDC, adjust gain for +10VDC output.
3. Reverse polarity of X input and adjust X_O to reduce the output error to ½ its original value, then readjust the gain to take out the remaining error.
4. Check the output offset with input grounded. If nonzero, repeat the above procedure until no errors remain.

DIVIDER

The divide mode utilizes the multiplier in a fed-back configuration where the Y input now controls the feedback factor. With X = full scale, the gain (V_O/Z) becomes unity after trimming. Reducing the X input reduces the feedback around the op amp by a like amount, thereby increasing the gain. This reciprocal relationship forms the basis of the divide mode. Accuracy and bandwidth decrease as the denominator decreases.

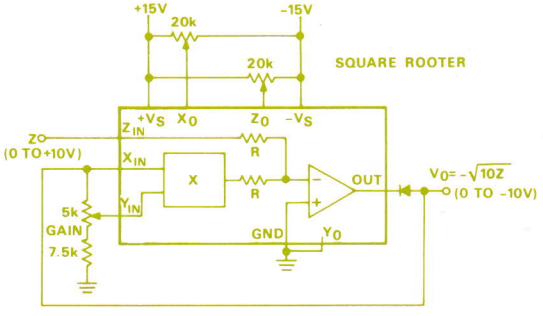


TRIM PROCEDURES

1. Set all pots at mid-scale.
2. With Z = 0V, trim Z_O to hold the output constant, as X is varied from -10VDC through -1VDC.
3. With Z = 0V, X = -10VDC, trim Y_O for 0VDC.
4. With Z = X or -X, trim X_O for the minimum worst-case variation as X is varied from -10VDC to -1VDC.
5. Repeat steps 2 and 3 if step 4 required a large initial adjustment.
6. With Z = X or -X, trim the gain for the closest average approach to ±10VDC output as X is varied from -10VDC to -3VDC.

SQUARE ROOTER

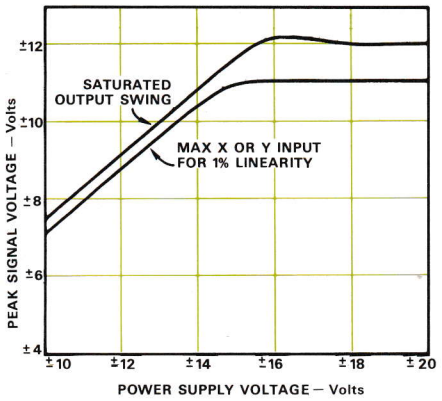
This mode is also a fed-back configuration with both the X and Y inputs tied to the op amp output through an external diode to prevent latchup. Accuracy, noise and frequency response are proportional to $\sqrt{Z}$, which implies a wider usable dynamic range than the divide mode.



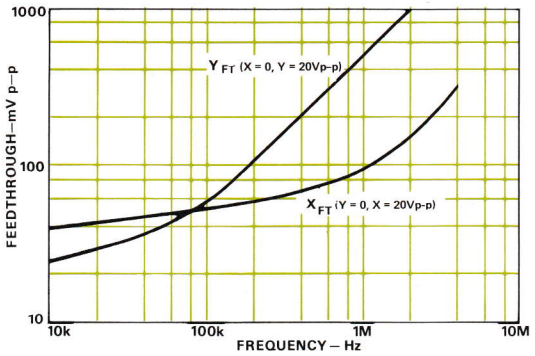
TRIM PROCEDURES

1. With Z = +0.1VDC, adjust Z_O for Output = -1.0VDC.
2. With Z = +10.0VDC, adjust Gain for Output = -10.0VDC.
3. With Z = +2.0VDC, adjust X_O for Output = -4.47 ±0.1VDC.
4. Repeat steps 2 and 3, if necessary. Repeat step 1.

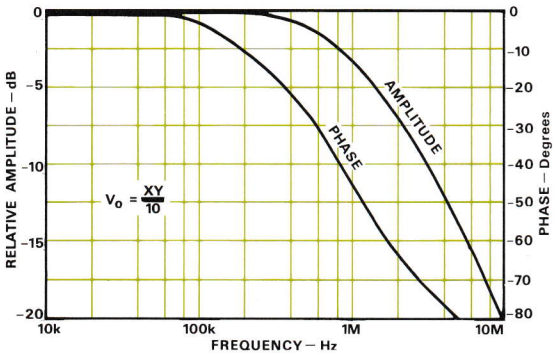
TYPICAL PERFORMANCE CHARACTERISTICS



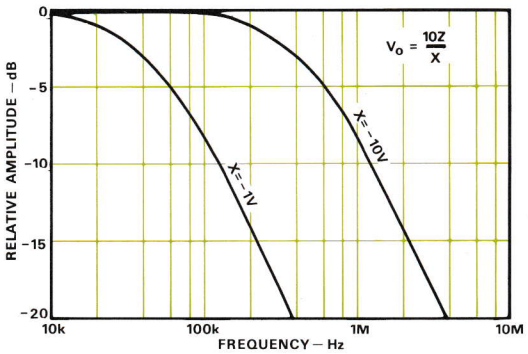
Allowable Signal Swing vs. Supply Voltage



Feedthrough vs. Frequency



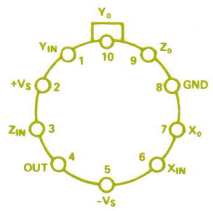
Closed Loop Frequency and Phase Response



Divide Mode Frequency Response

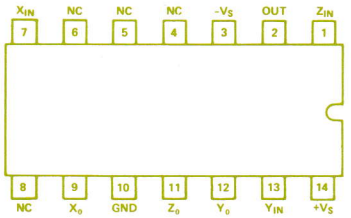
PIN CONFIGURATION & DIMENSIONS
(In Inches)

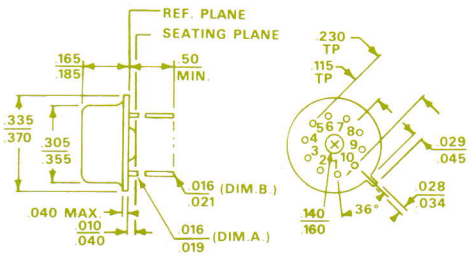
AD533H
TO-100

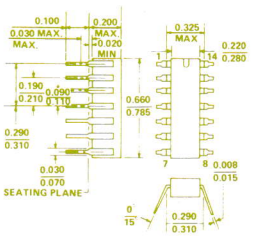


TOP VIEW

AD533D
TO-116







ORDERING GUIDE

MODEL	MULT. ERROR (Max @ +25°C)	TEMP. RANGE	ORDER NUMBER
AD533J	±2.0%	0 to +70°C	AD533JH*
			AD533JD†
AD533K	±1.0%	0 to +70°C	AD533KH
			AD533KD
AD533L	±0.5%	0 to +70°C	AD533LH
			AD533LD
AD533S	±1.0%	−55 to +125°C	AD533SH
			AD533SD

*TO-100 metal can package
†TO-116 ceramic DIL package

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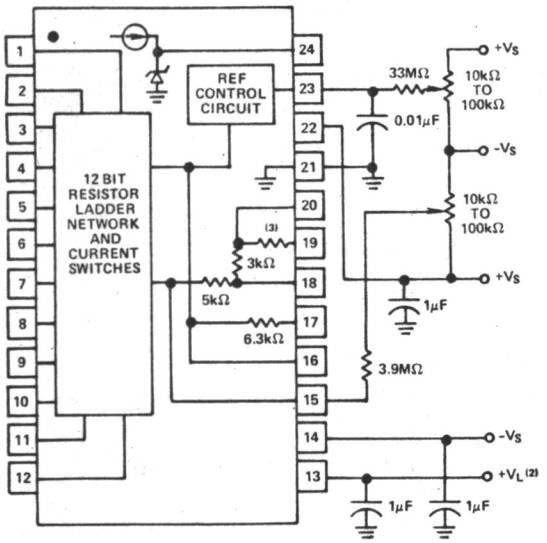


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

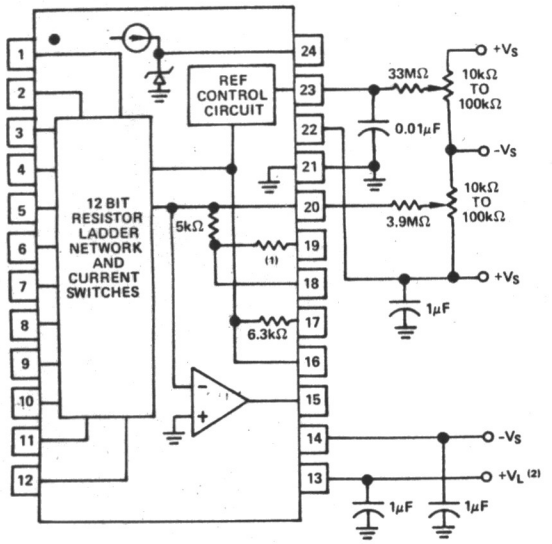


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

NOTES:

1. 3kΩ for CCD models. 5kΩ for CBI models.
2. If connected to $+V_S$ which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.

PIN CONFIGURATION

24 LEAD DUAL IN-LINE PACKAGE

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1(MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)

I Models	Pin #	V Models
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref Input	16	Ref Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
$6.3V_{REF}$ Out	24	$6.3V_{REF}$ Out

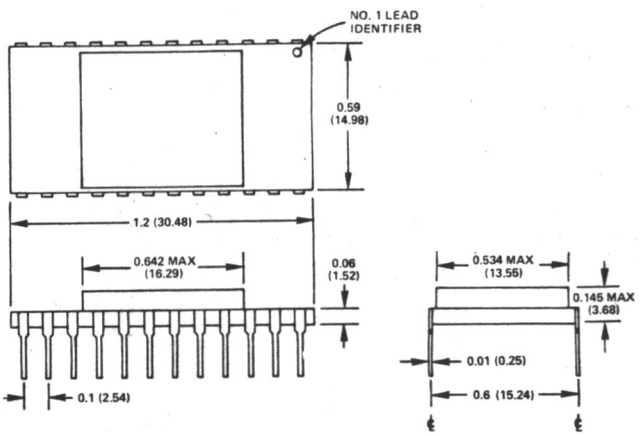


Figure 3. Outline Dimensions (Dimensions shown in inches and (mm))

AD DAC80 ORDERING GUIDE

MODEL	INPUT CODE	OUTPUT MODE	SUPPLY RANGE
AD DAC80-CBI-V	Binary	Voltage	Normal
AD DAC80-CBI-I	Binary	Current	Normal
AD DAC80-CCD-V	Binary Coded Decimal	Voltage	Normal
AD DAC80-CCD-I	Binary Coded Decimal	Current	Normal
AD DAC80Z-CBI-V	Binary	Voltage	Extended
AD DAC80Z-CBI-I	Binary	Current	Extended
AD DAC80Z-CCD-V	Binary Coded Decimal	Voltage	Extended
AD DAC80Z-CCD-I	Binary Coded Decimal	Current	Extended

Am25LS2521
Eight-Bit Equal-To Comparator

DISTINCTIVE CHARACTERISTICS

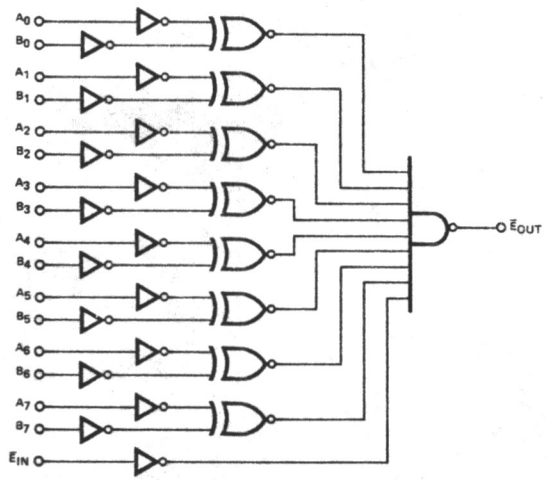
- 8-bit byte oriented equal comparator
- Cascadable using $\overline{E}_{IN}$
- High-speed, Low-Power Schottky technology
- t_{pd} A • B to $\overline{E}_{OUT}$ in 9ns
- Standard 20-pin package
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

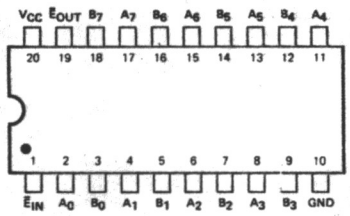
The Am25LS2521 is an 8-bit "equal to" comparator capable of comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{E}_{IN}$ produces an active LOW on the output $\overline{E}_{OUT}$.

The logic expression for the device can be expressed as: $\overline{E}_{OUT} = \overline{(A_0 \odot B_0)\ (A_1 \odot B_1)\ (A_2 \odot B_2)\ (A_3 \odot B_3)\ (A_4 \odot B_4)\ (A_5 \odot B_5)\ (A_7 \odot B_7)\ E_{IN}}$. It is obvious that the expression is valid where $A_0 - A_7$ and $B_0 - B_7$ are expressed as either assertions or negations. This is also true for pair of terms i.e. A_0 can be compared with B_0 at the same time $\overline{A}_1$ is compared with $\overline{B}_1$. It is only essential that the polarity of the paired terms be maintained.

LOGIC DIAGRAM

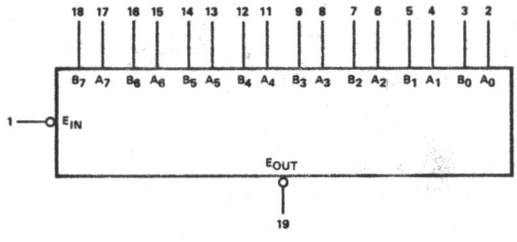


CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	MIN. = 4.75V	MAX. = 5.25V
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440µA	MIL	2.5			Volts
				COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V		A_i, B_i			−0.36	mA
				$\overline{E}$			−0.72	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		A_i, B_i			20	µA
				$\overline{E}$			40	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V		A_i, B_i			0.1	mA
				$\overline{E}$			0.2	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				27	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{E}$ = GND, all other inputs and outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERIS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description
t_{PLH} / t_{PHL}	A_i or B_i to $\overline{Equal}$
t_{PLH} / t_{PHL}	$\overline{E}$ to $\overline{Equal}$

SWITCHING CHARACTERIS OVER OPERATING RANGE

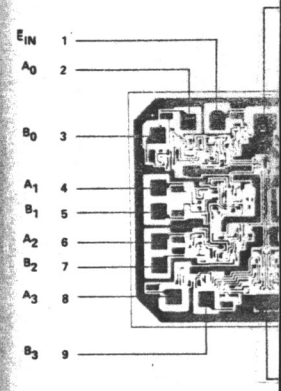
Parameters	Descri
t_{PLH} / t_{PHL}	A_i or B_i to $\overline{Equal}$ Output
t_{PLH} / t_{PHL}	$\overline{E}$ to $\overline{Equal}$ Output

*AC performance over the operating te

DEFINITION OF FUNCTIONAL

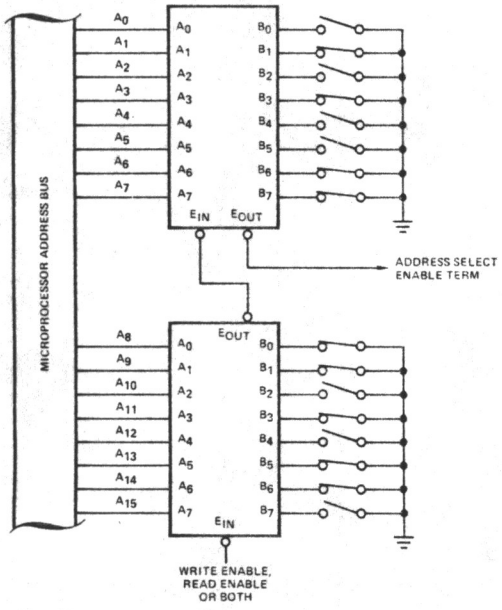
A_0–A_7	A input to comparato
B_0–B_7	B input to comparato
$\overline{E}_{IN}$	Enable active LOW
$\overline{E}_{OUT}$	$\overline{EQUAL}$ output active

Metallization an



DIE SIZE 0.0

APPLICATION



MAX. $\overline{\text{ENABLE}}$ (HIGH-to-LOW) DELAY OVER 16-BITS
(Commercial Range)

t_{PHL}	A_i or B_i to $\overline{E}_{OUT}$	19ns
t_{PHL}	$\overline{E}_{IN}$ to $\overline{E}_{OUT}$	12.5ns
Total		31.5ns

MICROPROCESSOR ENABLE CONTROLLED, SELECTABLE, ADDRESS DECODER

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2521PC
Hermetic DIP	0°C to +70°C	AM25LS2521DC
Dice	0°C to +70°C	AM25LS2521XC
Hermetic DIP	−55°C to +125°C	AM25LS2521DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS2521FM
Dice	−55°C to +125°C	AM25LS2521XM

XR-2207/2307

Voltage-Controlled Oscillator

OCTOBER 1973

VOLTAGE CONTROLLED OSCILLATOR

The XR-2207/2307 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

As shown in Figure 1, the circuit is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

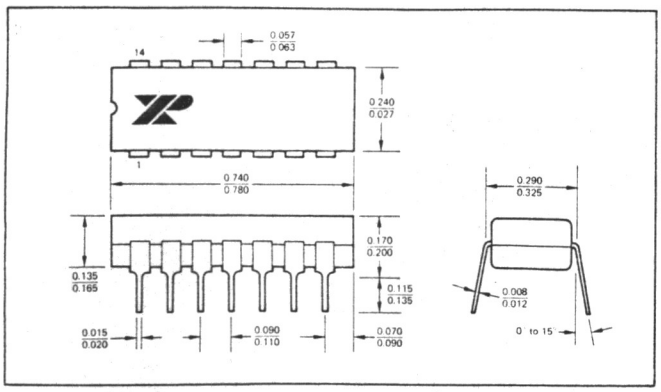
FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Adjustable Duty Cycle (0.1% to 99.9%)
Two or Four Level FSK Capability
Wide Sweep Range (1000:1 Min)
Logic Compatible Input and Output Levels
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.15%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

FSK Generation
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
FM and Sweep Generation

PACKAGE INFORMATION



ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	5 mW/°C
Plastic package	625 mW
Derate above +25°C	5 mW/°C
Total Timing Current (pins 4 through 7)	10 mA
Temperature Range	
Operating	
XR-2207M	−55°C to +125°C
XR-2207/2307C	0°C to +75°C
Storage	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM

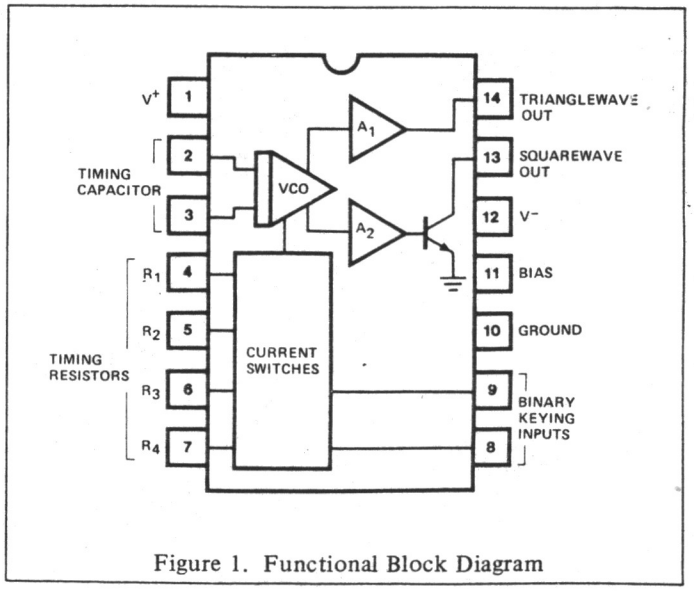


Figure 1. Functional Block Diagram

EXAR INTEGRATED SYSTEMS, INC.
750 Palomar Avenue, Sunnyvale, California 94086 (408) 732-7970 TWX 910-339-9233

ELECTRICAL CHARACTERISTICS

PARAMETERS	XR-2207			XR-2307			XR-2307C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Test Conditions: Test Circuit of Figure 2, $V^+ = V^- = 6V$, $T_A = +25°C$, C = 5000 pF, R_3 = 20 kΩ, Binary Inputs grounded, S_1 and S_2 closed unless otherwise specified.											
GENERAL CHARACTERISTICS											
Supply Voltage											
Single Supply	8		26	8		26	8		26	V	See Figure 3
Split Supplies	±4		±13	±4		±13	±4		±13	V	
Supply Current											
Single Supply		5	7		5	7		5	8	mA	Measured at pin 1, S_1, open, see Figure 3
Split Supplies											
Positive		5	7		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open
Negative		4	6		4	6		4	7	mA	Measured at pin 12, S_1, S_2 open
OSCILLATOR SECTION – FREQUENCY CHARACTERISTICS											
Upper Frequency Limit	0.5	1.0		0.5	1.0		0.5	1.0		MHz	C = 500 pF, R_3 = 2 kΩ
Lowest Practical Operating Frequency		0.01			0.01			0.01		Hz	C = 50 μF, R_3 = 2 MΩ
Frequency Accuracy		±1	±3		±1	±4		±1	±5	%of f_o	
Frequency Matching		0.5			0.5			0.5		%of f_o	
Frequency Stability											
Temperature		20	50		20	100		30		ppm/°C	$0° < T_A < 75°C$
Power Supply		0.15			0.15			0.15		%/V	
Sweep Range	1000:1	3000:1		1000:1	3000:1			1000:1		f_H/f_L	R_3 = 1.5 kΩ for f_{H1} R_3 = 2 MΩ for f_L
Sweep Linearity											
10:1 Sweep		1	2		1	3		1.5	5	%	C = 5000 pF
100:1 Sweep		3			3			3			f_H = 10 kHz, f_L = 1 kHz
1000:1 Sweep		5			5			5			f_H = 30 kHz, f_L = 300 Hz f_H = 100 kHz, f_L = 100 Hz
FM Distortion		0.1			0.1			0.1		%	±10% FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	1.5		2000	kΩ	See Characteristic Curves
Impedance at Timing Terminals		75			75			75		Ω	Measured at pins 4, 5, 6, or 7 with Timing Resistor of 20 kΩ
DC Level at Timing Terminals		10			10			10		mV	
BINARY KEYING INPUTS											
Switching Threshold	1.4	2.2	2.8	1.4	2.2	2.8	1.4	2.2	2.8	V	Measured at pins 8 and 9, Refer to pin 10.
Input Impedance		5			5			5		kΩ	
OUTPUT CHARACTERISTICS											
Triangle Output											
Amplitude	4	6		4	6		4	6		V_{pp}	Measured at pin 13
Impedance		10			10			10		Ω	
DC Level		+100			+100			+100		mV	
Linearity		0.1			0.1			0.1		%	Referenced to pin 10
Squarewave Output											
Amplitude	11	12		11	12		11	12		V_{pp}	Measured at pin 13, S_5 closed
Saturation Voltage		0.2	0.4		0.2	0.4		0.2	0.4	V	
Rise Time		200			200			200		nsec.	Referenced to pin 12 $C_L \leq 10$ pF
Fall Time		20			20			20		nsec.	$C_L \leq 10$ pF

XR-2206

R.ohm QUALITY · RELIABILITY

(ORIGINAL)

Monolithic Function Generator

OCTOBER 1975

MONOLITHIC FUNCTION GENERATOR

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp and pulse waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The XR-2206 is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage with very little affect on distortion.

As shown in Figure 1, the monolithic circuit is comprised of four functional blocks: a voltage-controlled oscillator (VCO); an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The internal current switches transfer the oscillator current to any one of the two external timing resistors to produce two discrete frequencies selected by the logic level at the FSK input terminal (pin 9).

FEATURES

- Low Sinewave Distortion (THD .5%) – insensitive to signal sweep
- Excellent Stability (20 ppm/°C, typ)
- Wide Sweep Range (2000:1, typ)
- Low Supply Sensitivity (0.01%/V, typ)
- Linear Amplitude Modulation
- Adjustable Duty-Cycle (1% to 99%)
- TTL Compatible FSK Controls
- Wide Supply Range (10V to 26V)

APPLICATIONS

- Waveform Generation
  Sine, Square, Triangle, Ramp
- Sweep Generation
- AM/FM Generation
- FSK and PSK Generation
- Voltage-to-Frequency Conversion
- Tone Generation
- Phase-Locked Loops

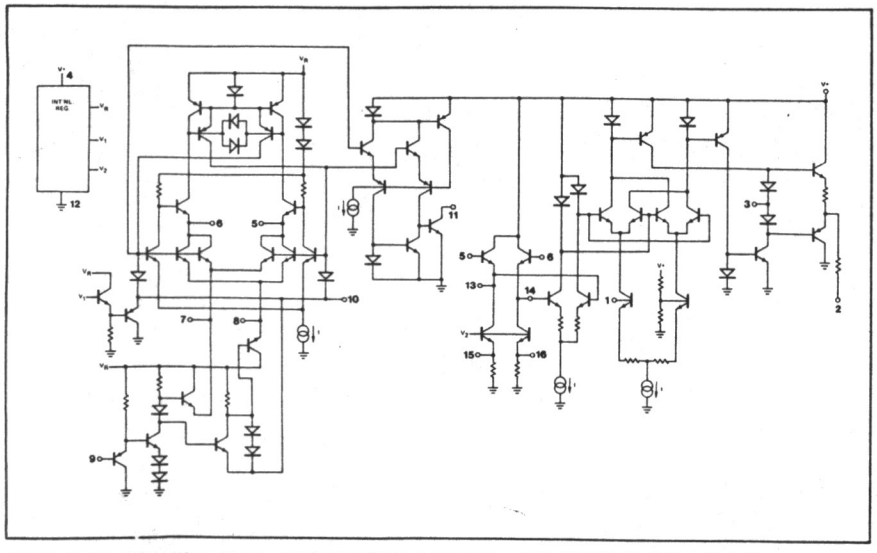
ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750 mW
Derate above 25°C	5 mW/°C
Total Timing Current	6 mA
Operating Temperature	
Storage Temperature	−65°C to +150°C

AVAILABLE TYPES

Part Number	Package Types (16 Pin DIP)	Operating Temperature Range
XR-2206M	Ceramic	−55°C to +125°C
XR-2206N	Ceramic	0°C to +75°C
XR-2206P	Plastic	0°C to +75°C
XR-2206CN	Ceramic	0°C to +75°C
XR-2206CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

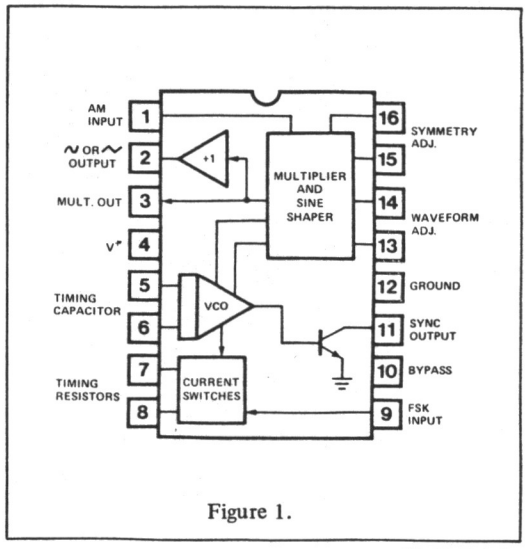


Figure 1.

EXAR INTEGRATED SYSTEMS, INC.
750 Palomar Ave., Sunnyvale, CA 94086
(408) 733-7700 TWX 910-339-9233

10-75 REV 1

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Fig. 2, $V^+ = 12V$, $T_A = 25°C$, $C = 0.01\ \mu F$, $R_1 = 100\ K\Omega$, $R_2 = 10\ K\Omega$ $R_3 = 25\ K\Omega$ unless otherwise specified. S_1 open for triangle, closed for sinewave.

CHARACTERISTICS	XR-2206M, XR-2206			XR-2206C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage								
Single Supply	10		26	10		26	V	
Split Supply	±5		±13	±5		±13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10\ K\Omega$
Oscillator Section								
Max. Operating Frequency	0.5	1		0.5	1		MHz	C=1000 pF, R_1=1 KΩ
Lowest Practical Frequency		0.01			0.01		Hz	C=50 μF, R_1=2 MΩ
Frequency Accuracy		±1	±4		±2		% of f_o	$f_0 = 1/R_1C$
Temperature Stability		±10	±50		±20		ppm/°C	$0°C \leq T_A \leq 75°C$, $R_1 = R_2 = 20\ K\Omega$
Supply Sensitivity		0.01	0.1		0.01		%	$V_{LOW} = 10V$, $V_{HIGH} = 20V$, $R_1 = R_2 = 20\ K\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1 KΩ f_L @ R_1 = 2 MΩ
Sweep Linearity								
10:1 Sweep		2			2		%	f_L = 1 kHz, f_H = 10 kHz
1000:1 Sweep		8			8		%	f_L = 100 Hz, f_H = 100 kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	μF	See Figure 5
Timing Resistors: R_1 & R_2	1		2000	1		2000	KΩ	
Triangle/Sinewave Output								See Note 1, Fig.
Triangle Output		160			160		mV/KΩ	Fig. 2 S_1 Open
Sinewave Output	40	60	80		60		mV/KΩ	Fig. 2 S_1 Closed
Max. Output Swing		6			6		Vpp	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sinewave Distortion								R_1 = 30 KΩ
Without Adjustment		2.5			2.5		%	See Figure 11.
With Adjustment		0.4	1.0		0.5	1.5	%	See Figure 12
Amplitude Modulation								
Input Impedance	50	100		50	100		KΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square Wave Output								Measured at Pin 11
Amplitude		12			12		Vpp	
Rise Time		250			250		nsec	C_L = 10 pF
Fall Time		50			50		nsec	C_L = 10 pF
Saturation Voltage		0.2	0.4		0.2	0.4	V	I_L = 2 mA
Leakage Current		0.1	20		0.1		μA	V_{11} = 12V
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See Section on Circuit Controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output Amplitude is inversely proportional to the resistance R_3 on Pin 3. See Figure 3

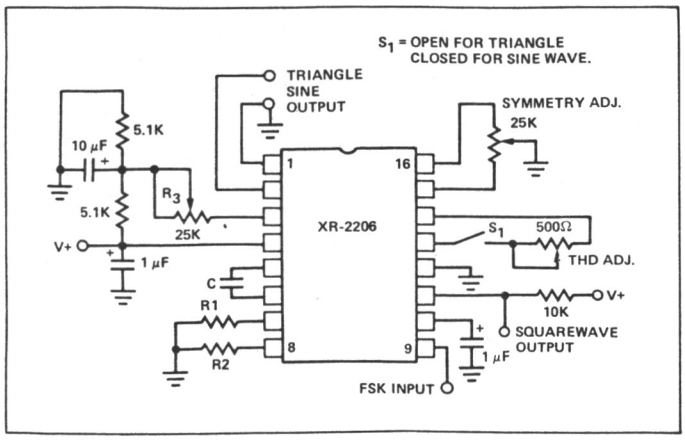


Figure 2. Basic Test Circuit

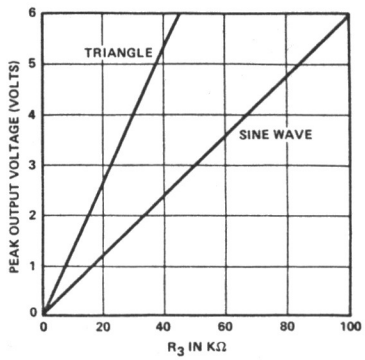


Figure 3. Output Amplitude as a Function of Resistor R_3 at Pin 3.

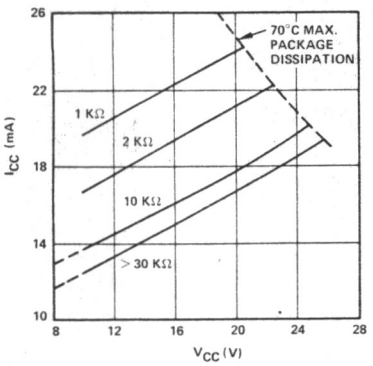


Figure 4. Supply Current vs Supply Voltage, Timing R

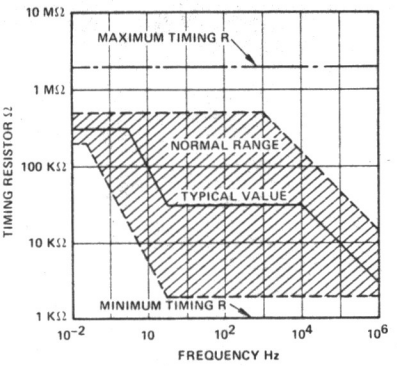


Figure 5. R vs Oscillation Frequency

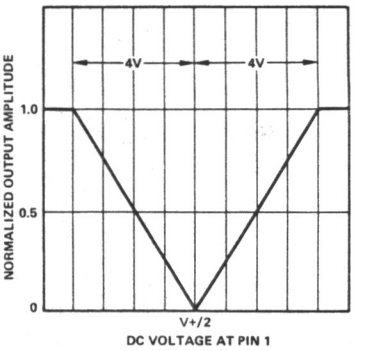


Figure 6. Normalized Output Amplitude vs DC Bias at AM Input (Pin 1).

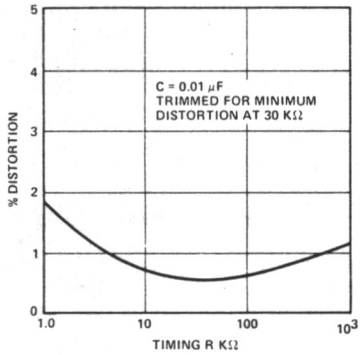


Figure 7. Trimmed Distortion vs Timing Resistor

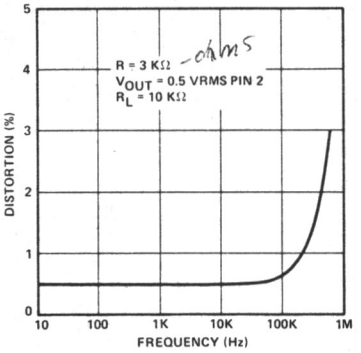


Figure 8. Signwave Distortion vs Operating Frequency With Timing Capacitors Varied

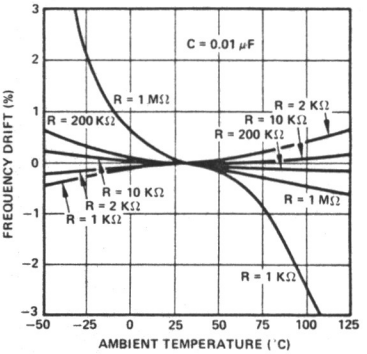


Figure 9. Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

FREQUENCY OF OPERATION:

The frequency of oscillation, f_o, is determined by the external timing capacitor C across pins 5 and 6, and by the timing resistor R connected to either pin 7 or pin 8. The frequency is given as

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R for a given frequency range are shown in Figure 5. Temperature stability is optimum for $4\ K\Omega < R < 200\ K\Omega$. Recommended values of C are from 1000 pF to 100 μF.

FREQUENCY SWEEP AND MODULATION

Frequency of oscillation is proportional to the *total* timing current I_T drawn from pin 7 or 8

$$f = \frac{320 I_T\ (mA)}{C\ (\mu F)} \text{ Hz}$$

Timing terminals (pins 7 or 8) are low impedance points and are internally biased at +3V, with respect to pin 12. Frequency varies linearly with I_T over a wide range of current values, from 1 μA to 3 mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in Figure 10. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC}\left[1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right] \text{ Hz}$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f / \partial V_C = -\frac{0.32}{R_C C} \text{ Hz/V}$$

NOTE: For safe operation of the circuit I_T should be limited to ≤ 3 mA.

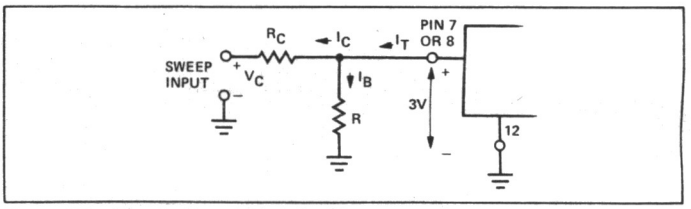


Figure 10. Circuit Connection for Frequency Sweep

OUTPUT CHARACTERISTICS:

Output Amplitude: Maximum output amplitude is inversely proportional to external resistor R_3 connected to Pin 3 (See Fig. 3). For sinewave output, amplitude is approximately 60 mV peak per KΩ of R_3; for triangle, the peak amplitude is approximately 160 mV peak per KΩ of R_3. Thus, for example, R_3 = 50 KΩ would produce approximately ±3V sinusoidal output amplitude.

Amplitude Modulation: Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 200 KΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within ±4 volts of $V^+/2$ as shown in Fig. 6. As this bias level approaches $V^+/2$, the phase of the output signal is reversed; and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB.

Note: AM control must be used in conjunction with a well-regulated supply since the output amplitude now becomes a function of V^+.

FREQUENCY-SHIFT KEYING

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing pins 7 and 8, respectively, as shown in Figure 13. Depending on the polarity of the logic signal at pin 9, either one or the other of these timing

resistors is activated. If pin 9 is open-circuited or connected to a bias voltage $\geq 2V$, only R_1 is active. Similarly, if the voltage level at pin 9 is $\leq 1V$, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2 as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at pin 9 is referenced to V^-.

OUTPUT DC LEVEL CONTROL

The dc level at the output (pin 2) is approximately the same as the dc bias at pin 3. In Figures 11, 12 and 13, pin 3 is biased mid-way between V^+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

SINEWAVE GENERATION

A) Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer R_1 at pin 7 provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$ and the

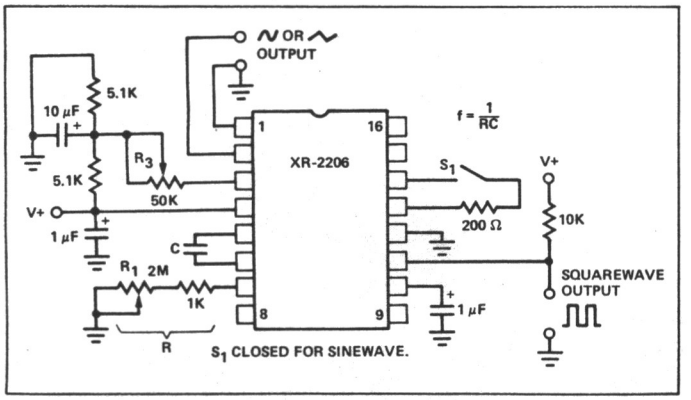


Figure 11. Circuit for Sinewave Generation Without External Adjustment. (See Fig. 3 for choice of R_3)

typical distortion (THD) is $< 2.5\%$. If lower sinewave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 11 can be converted to split supply operation simply by replacing all ground connections with V^-. For split supply operation, R_3 can be directly connected to ground.

B) With External Adjustment

The harmonic content of sinusoidal output can be reduced to $\approx 0.5\%$ by additional adjustments as shown in Figure 12 The potentiometer R_A adjusts the sine-shaping resistor;

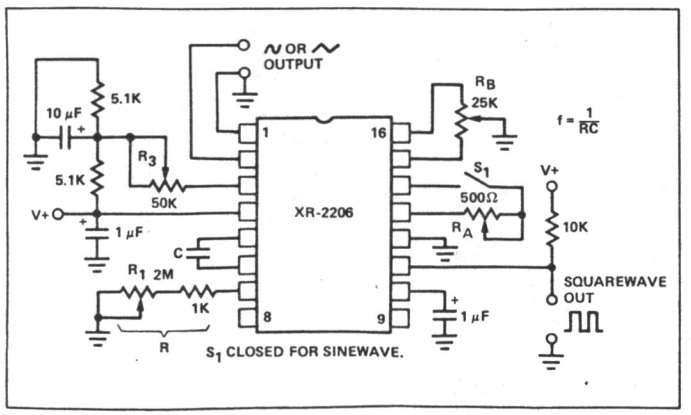


Figure 12. Circuit for Sinewave Generation With Minimum Harmonic Distortion. (R_3 Determines output Swing – See Fig. 3)

and R_B provides the fine-adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at mid-point and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

TRIANGLE WAVE GENERATION

The circuits of Figures 11 and 12 can be converted to triangle wave generation by simply open circuiting pins 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sinewave output.

FSK GENERATION

Figure 13 shows the circuit connection for sinusoidal FSK signal generation. Mark and space frequencies can be independently adjusted by the choice of timing resistors R_1 and R_2; and the output is phase-continuous during transitions. The keying signal is applied to pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^-.

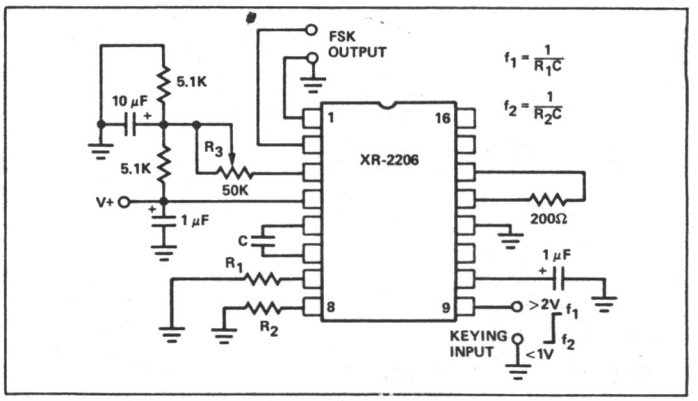


Figure 13. Sinusoidal FSK Generator

PULSE AND RAMP GENERATION

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (pin 9) is shorted to the square-wave output (pin 11); and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive and negative going output waveforms. The pulse-width and the duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1 KΩ to 2 MΩ.

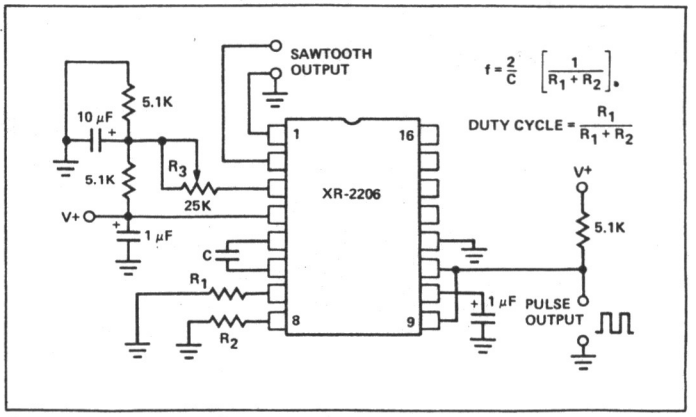


Figure 14. Circuit for Pulse and Ramp Generation

XR-215

Monolithic Phase-Locked Loop

JUNE 1974

The XR-215 is a highly versatile monolithic phase-locked loop (PLL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

Figure 1 contains a functional block diagram of the XR-215 monolithic PLL system. The circuit consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and a high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals.

The VCO section has frequency sweep, on-off keying, sync, and digital programming capabilities. Its frequency is highly stable and is determined by a single external capacitor. The operational amplifier can be used for audio preamplification in FM detector applications; or, as a high speed sense amplifier (or comparator) in FSK demodulation.

FEATURES

Wide Frequency Range: 0.5 Hz to 35 MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
DTL, TTL and ECL Logic Compatibility
Wide Dynamic Range: 300 μV to 3V
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from ±1% to ±50%
High-Quality FM Detection: Distortion 0.15%
Signal/Noise 65dB

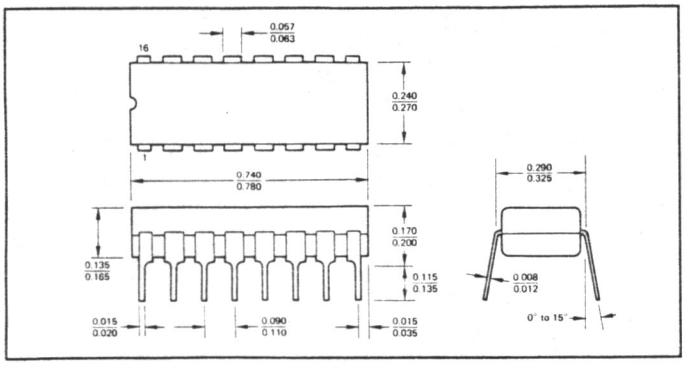
APPLICATIONS

FM Demodulation
Frequency Synthesis
FSK Coding/Decoding (MODEM)
Tracking Filters
Signal Conditioning
Tone Decoding
Data Synchronization
Telemetry Coding/Decoding
FM, FSK and Sweep Generation
Crystal Controlled Detection
Wideband Frequency Discrimination
Voltage-to-Frequency Conversion

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Temperature	
Operating	0°C to +75°C
Storage	−65°C to +150°C

PACKAGE INFORMATION (ceramic)



FUNCTIONAL BLOCK DIAGRAM

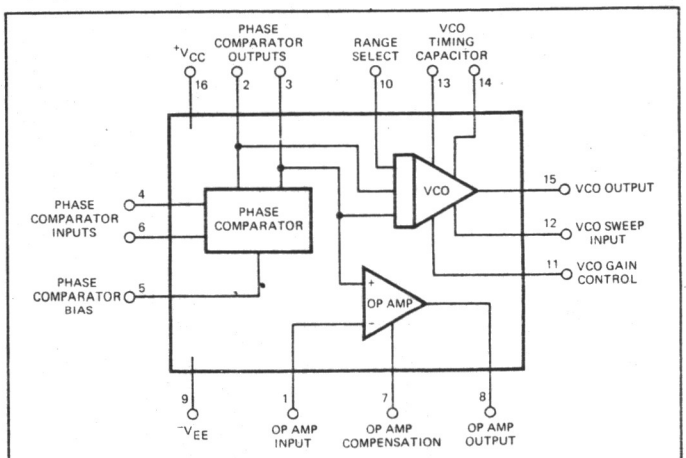


Figure 1. XR-215 Functional Block Diagram

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ELECTRICAL SPECIFICATIONS

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
I – General Characteristics **Test Conditions:** V^+ = 12V (single supply), T_A = 25°C, Test Circuit of Figure 2 with C_0 = 100 pF, (silver-mica) S_1, S_2, S_5, closed, S_3, S_4 open unless otherwise specified.					
Supply Voltage:					
Single Supply	5		26	V dc	See Figure 2
Split Supply	±2.5		±13	V dc	See Figure 3
Supply Current	8	11	15	mA	See Figure 2
Upper Frequency Limit	20	35		MHz	See Figure 2, S_1 open, S_4 closed
Lowest Practical Operating Frequency		0.5		Hz	C_0 = 500 μF
VCO Section:					
Stability:					
Temperature		250	600	ppm/°C	See Figure 2, $0°C \leq T_A \leq 75°C$
Power Supply		0.1		%/V	$V^+ > 10V$
Sweep Range	5:1	8:1			S_3 closed, S_4 open, $0 < V_S < 6V$ See Figure 9, C_0 = 2000 pF
Output Voltage Swing	1.5	2.5		V_{p-p}	S_5 open
Rise Time		20		ns	10 pF to ground at Pin 15
Fall Time		20		ns	
Phase Comparator Section:					
Conversion Gain		2		V/rad	$V_{in} > 50$ mV rms (See characteristic curves)
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		20	100	mV	Measured across Pins 2 and 3 V_{in} = 0, S_5 open
Op Amp Section:					
Open Loop Voltage Gain	66	80		dB	S_2 open
Slew Rate		2.5		V/μ sec	A_V = 1
Input Impedance	0.5	2		MΩ	
Output Impedance		2		kΩ	
Output Swing	7	10		V_{p-p}	R_L = 30 kΩ from Pin 8 to ground
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	
II – Special Applications A) FM Demodulation: **Test Conditions:** Test circuit of Figure 4, V^+ = 12V, input signal = 10.7 MHz FM with Δf = 75 kHz, f_{mod} = 1 kHz					
Detection Threshold		0.8	3	mV rms	50Ω source
Demodulated Output Amplitude	250	500		mV rms	Measured at Pin 8
Distortion (THD)		0.15	0.5	%	
AM Rejection		40		dB	V_{in} = 10 mV rms, 30% AM
Output Signal/Noise	55	65		dB	
B) Tracking Filter **Test Conditions:** Test circuit of Figure 5, V^+ = 12V, f_o = 1 MHz, V_{in} = 100 mV rms, 50Ω source					
Tracking Range (% of f_o)	±30	±50			See Figures 5 and 25
Discriminator Output $\frac{\Delta V_{out}}{\Delta f/f_o}$		50		mV/%	Adjustable – See applications information

XR-205

Monolithic Waveform Generator

JUNE 1974

The XR-205 is a highly versatile, monolithic waveform generator designed for diverse applications in communication and telemetry equipment, as well as in systems design and testing. It is a self-contained, totally monolithic signal generator that provides sine, square, triangle, ramp and sawtooth output waveforms, which can be both amplitude and frequency modulated.

Figure 1 shows the functional block diagram of the monolithic waveform generator. The circuit has three separate sections: a voltage-controlled oscillator (VCO) which generates the basic periodic waveforms; a balanced modulator which provides amplitude or phase modulation; a buffer amplifier section which provides a low impedance output with high current drive capability.

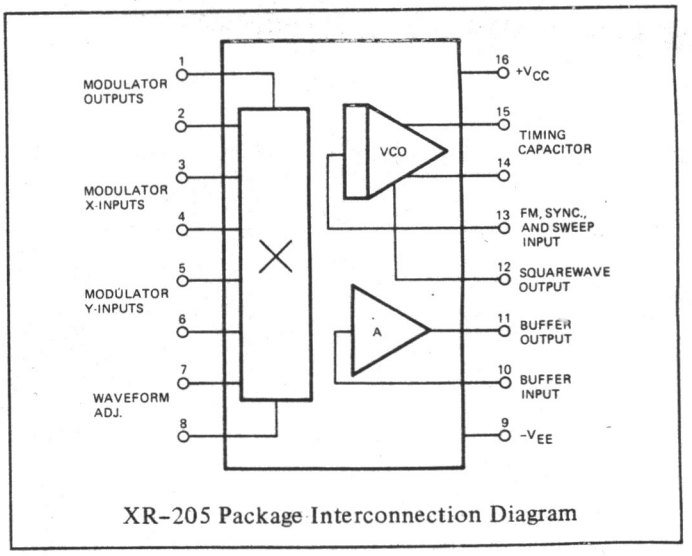
APPLICATIONS

1. Waveform Generation
   Sinewave
   Triangle
   Square
   Sawtooth
   Ramp
   Pulse
2. AM Generation
   Double Sideband
   Suppressed Carrier
   Crystal-Controlled
3. FM Generation
4. Sweep Generation
5. Tone Burst Generation
6. Simultaneous AM/FM
7. Frequency-Shift Keyed (FSK) Signal Generation
8. Phase-Shift Keyed (PSK) Signal Generation
9. On-Off Keyed Oscillation
10. Clock Generation

ABSOLUTE MAXIMUM RATINGS

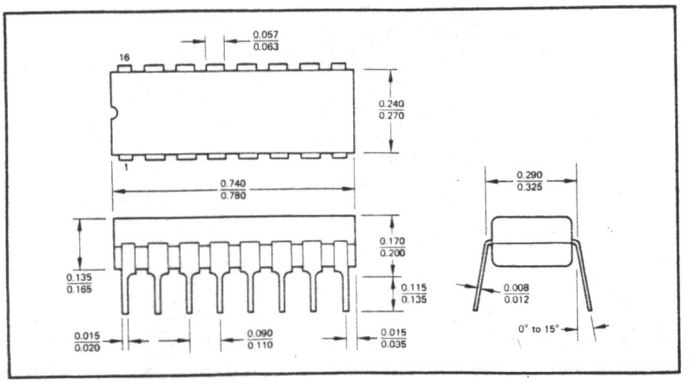
Power Supply	26 volts
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Temperature	
Operating	0°C to +75°C
Storage	−65°C to +150°C

SYSTEM BLOCK DIAGRAM



XR-205 Package Interconnection Diagram

PACKAGE INFORMATION (ceramic)



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ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = 12V (single supply) $T_A = 25°C$, f = 10 kHz, $R_L = 3\ k\Omega$, unless otherwise specified.

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
I – General Characteristics					
Supply Voltage:					
Single Supply	8		26	V dc	See Figure 1
Split Supply	±5		±13	V dc	See Figures 2, 3 and 4
Supply Current	8	10	12	mA	w/o buffer amp
Frequency Stability:					
Power Supply		0.2	0.5	%/V	$\|V_{CC} - V_{EE}\| > 10V$
Temperature		300	600	ppm/°C	Sweep input open circuit
Frequency Sweep Range	7:1	10:1			See Figure 6
Output Swing:					
Single Ended	2	3		V pp	Measured at pin 1 or 2
Differential	4	6		V pp	Measured across 1 and 2
Output Diff. Offset Voltage		0.1	0.4	V dc	Measured across 1 and 2
Amplitude Control Range		60		dB	Controlled by R_q (see Figure 1)
Buffer Amplifier Output Resistance		50		ohms	$R_L = 750\Omega$
Output Current Swing	±6	±10		mA	
II – Output Waveforms					
Sinusoidal:					
Upper Frequency Limit	2	4		MHz	Measured at Pin 11
Peak Output Swing	2	3		V.pp	See Figure 1, S_1, S_3
Distortion (THD)		2.5	4	%	closed S_2 open
Triangle:					
Peak Swing	2	3		V pp	See Figure 1, S_1, S_2
Non-Linearity		±1		%	open S_3 closed
Asymmetry		±1		%	f = 10 kHz
Sawtooth:					
Peak Swing	2	3		V pp	See Figure 1, S_2 closed;
Non-Linearity		1.5		%	S_2 and S_3 closed
Ramp:					
Peak Swing	1	1.4		V pp	See Figure 1, S_2 and S_3 open
Non-Linearity		1		%	pin 10 shorted to pin 15
Squarewave (Low Level):					
Output Swing	0.5	0.7		V pp	See Figure 1, S_2 and S_3 open,
Duty Cycle Asymmetry		±1	±4	%	pin 10 shorted to pin 12
Rise Time		20		ns	10 pF connected from pin 11
Fall Time		20		ns	to ground
Squarewave (High Level):					
Peak Swing	2	3		V pp	See Figure 3, S_2 open
Duty Cycle Asymmetry		±1	±4	%	
Rise Time		80		ns	10 pF connected from pin 11
Fall Time		60		ns	to ground
Pulse Output:					
Peak Swing	2	3		V pp	See Figure 3, S_2 closed
Rise Time		80		ns	
Fall Time		60		ns	
Duty Cycle Range		20–80		%	Adjustable (see Figure 11)
III – Modulation Characteristics (sine, triangle and squarewave):					
Amplitude Modulation:					
Double Sideband					
Modulation Range		0–100		%	See Figure 2
Linearity		0.5		%	for 30% modulation
Sideband Symmetry		1.0		%	
Suppressed Carrier					
Carrier Suppression		52		dB	f < 1 MHz
Frequency Modulation:					
Distortion		0.3		%	See Figure 2 (±10 frequency deviation)

ALL

XR-2208

Operational Multiplier

JUNE 1974

MONOLITHIC OPERATIONAL MULTIPLIER

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extration. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100 MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability. The XR-2208 operate over a 0°C to 75°C temperature range. The XR-2208M is specified for operation over the military temperature range of −55°C to +125°C

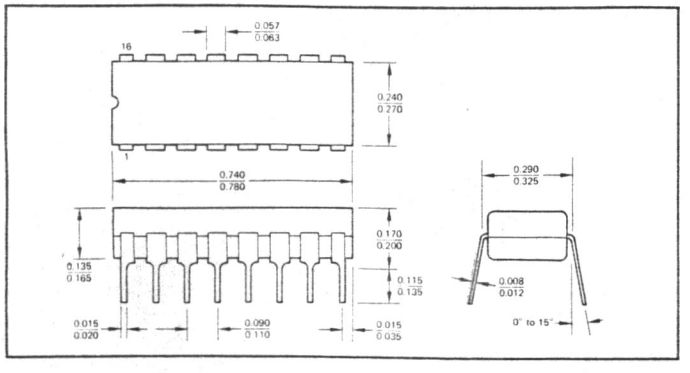
FEATURES

Maximum Versatility
  Independent Multiplier, Op Amp, and Buffer
Excellent Linearity (0.3% typ.)
Wide Bandwidth
  3 dB B.W. – 8 MHz typ.
  3° Phase Shift B.W. – 1.2 MHz typ.
  Transconductance B.W. – 100 MHz typ.
Simplified Offset Adjustments
Wide Supply Voltage Range (±4.5V to ±16V)

ABSOLUTE MAXIMUM RATINGS

Power Supply V^+	+18 Volts
V^-	−18 Volts
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mW/°C
Plastic Package	625 mW
Derate above +25°C	5.0 mW/°C
Temperature	
Operating	
XR-2208/2208C	0°C to +75°C
XR-2208M	−55°C to +125°C
Storage	−65°C to +150°C

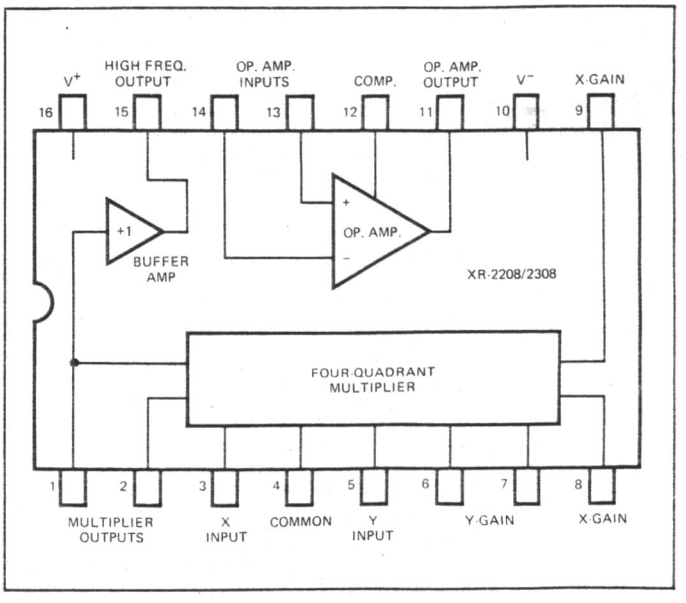
PACKAGE OUTLINE



APPLICATIONS

Analog Computation
  Multiplication
  Division
  Squareing
  Square-Root
Signal Processing
  AM Generation
  Frequency Doubling
  Frequency Translation
  Synchronous AM Detection
  Triangle-to-Sinewave Converter
  AGC Amplifier
  Phase Detector
Phase-Locked Loop (PLL) Applications
  Motor Speed Control
  Precision PLL
  Carrier Detection
  Phase-Locked AM Demodulation

FUNCTIONAL BLOCK DIAGRAM



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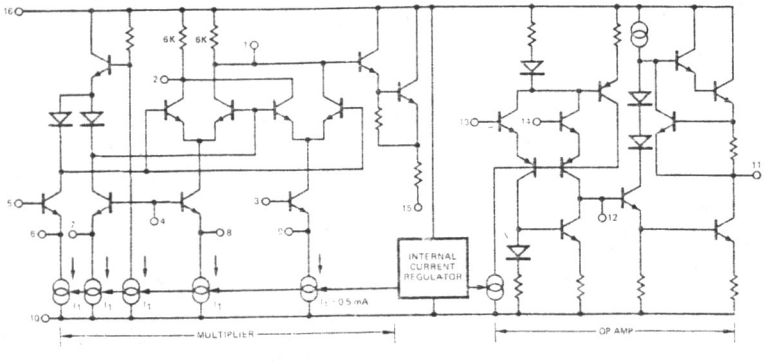
ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = ±15V, T_A = 25°C, unless otherwise specified.

CHARACTERISTICS	XR-2208/XR-2208M			XR-2208C			UNITS	FIGURES	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
I. GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	V dc		See Figure 11
Supply Current		4	7		5	8	mA	2	Measured at Pin 16
II. MULTIPLIER SECTION									
Non-linearity									No external offset rim
(Output Error in % of Full Scale)		0.3	0.5		0.5	1.0	%	3	V_y = ±10V, −10V < V_x < +10V
		0.3	0.5		0.5	1.0	%		V_x = ±10V, −10V < V_y < +10V
		0.7	1.0		0.8		%		$T_{LOW} \leq T_A \leq T_{HIGH}$ (Note 1)
									f = 50 Hz
Feedthrough									
a) With Offset Adj.									
X-input		45	80		70	120	mVp-p		V_X = 20 Vp-p V_y = 0
Y-input		60	100		90	150	mVp-p		V_y = 20 Vp-p, V_X = 0
b) No Offset Adj.									
X-input		120			200		mVp-p		V_X = 20 Vp-p, V_X = 0
Y-input		120			200		mVp-p		V_y = 20 Vp-p, V_X = 0
Temperature Coefficient of Scale Factor		±0.07			±0.07		%/°C		$T_{LOW} \leq T_A \leq T_{HIGH}$ (Note 1)
Input Bias Current									
X, Y input		2	6		3	8	μA	2	I_3, I_5 of Figure 2
Common input		4	12		6	16	μA	2	I_4 of Figure 2
Input Resistance	0.5	1.0			1.0		MΩ	2	Measured looking into Pin 3 or Pin 5
Output Offset Voltage		50	80		80	140	mV	2	Measured across Pins 1 and 2
Avg. Temp. Drift		0.5			0.5		mV/°C		$T_{LOW} \leq T_A \leq T_{HIGH}$
Dynamic Response								5	See Definition Section
3-dB Bandwidth									
X-input	6	8		6	8		MHz		
Y-input	3	4		3	4		MHz		
3° Phase-Shift Bandwidth		1.2			1.2		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		6			6		kΩ		Measured looking into pins 1 or 2
III. BUFFER AMPLIFIER									
Output Impedance		200			200		Ω	5	Measured looking into Pin 15
Gain		1.0			1.0				
IV. OPERATIONAL AMPLIFIER									
Input Offset Voltage		1	3		2	6	mV	6	R_S < 50Ω
Temperature Coefficient of Input Offset Voltage		6	20		9	30	μV/°C		$T_{LOW} \leq T_A \leq T_{HIGH}$
Input Offset Current		4	75		10	100	nA	6	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	6	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	6	$R_L \geq$ 2K, V_o = ±10V, f = 20 Hz
Differential Input Resistance	0.5	3			3		MΩ	6	
Output Voltage Swing	±10	±12		±10	±12		V		$R_L \geq$ 2K, $T_{LOW} \leq T_A \leq T_{HIGH}$
Input Common Mode Range	+12 −10	+14 −12		+12 −10	+14 −12		V	6	
Common Mode Rejection	70	90		70	90		dB	6	f = 20 Hz
Output Resistance		2			2		kΩ	6	
Slew Rate		0.5			0.5		V/μs	7	Gain = 1, $R_L \geq$ 2K, $C_L \leq$ 100 pF C_C = 20 pF
Power Supply Sensitivity		30			30		μV/V	6	$R_S \leq$ 10K

Note 1: T_{LOW} = −55°C, T_{HIGH} = +125°C for XR-2208M T_{LOW} = 0°C, T_{HIGH} = +75°C for XR-2208/XR-2208C



CAUTION

When using only the op amp or only the multiplier section of the XR-2208, the input terminals to the unused section *must be grounded*. Thus, when using the multiplier section alone, ground pin 13 and 14; when using the op amp section alone, ground pins 3, 4 and 5.

Figure 1. XR-2208/2208C Operational Multiplier Equivalent Circuit Schematic

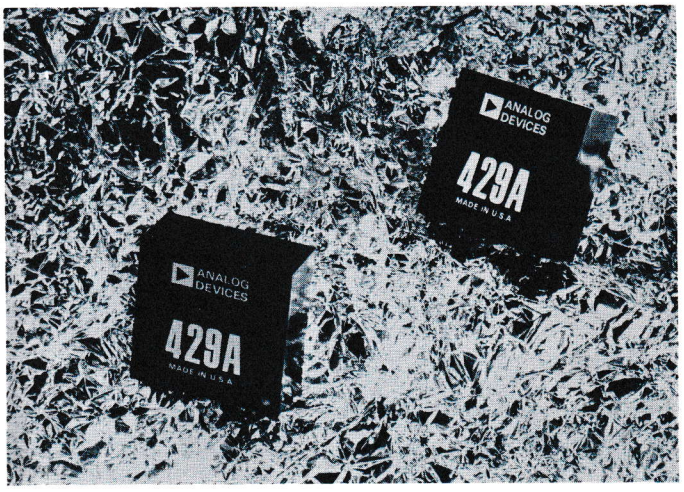
ANALOG DEVICES

Accurate, Wideband, Multiplier/Divider

MODEL 429

FEATURES:
- 1.0%/0.5% Accuracy without Trimming (429A/B)
- Low Drift to 1.0mV/°C max
- Wideband — 10MHz
- 0.2% Nonlinearity max (429B)
- External Amplifiers not Required

APPLICATIONS:
- Fast Divider
- Modulation and Demodulation
- Phase Detection
- Instrumentation Calculations
- Analog Computer Functions
- Adaptive Process Control
- Trigonometric Computations



GENERAL DESCRIPTION

The Model 429, an extremely fast multiplier/divider, should be considered if bandwidth, temperature coefficient, or accuracy are critical parameters. Based on the transconductance principle to achieve high speed, the model 429 offers a unique combination of features, those being ½% max error (429B) and 10MHz small signal bandwidth.

Both models 429A and 429B are internally trimmed achieving max errors of 1.0% and 0.5% respectively. By fine trimming the offset and feedthrough with external trim potentiometers typical performance may be improved to 0.5% for the 429A and 0.2% for the 429B.

In addition to high accuracy and high bandwidth, the model 429 offers exceptionally good stability for changes in ambient temperature. Model 429B is 100% temperature tested in order to guarantee an overall accuracy temperature coefficient of only 0.04%/°C max. Additionally, offset drift is held to only 1mV/°C max. To satisfy OEM requirements of low cost, the 429 uses transconductance principles with the latest design techniques and components to achieve guaranteed performance at competitive prices.

MULTIPLICATION ACCURACY

Multiplication accuracy is generally specified as a percentage of full scale output. This implies that error is independent of signal level. However, for signal levels less than 2/3 of full scale, error tends to decrease roughly in proportion to the input signal. A good approximation of error behavior is:

$f(X, Y) \cong |X| \epsilon_x + |Y| \epsilon_y$, where ϵ_x and ϵ_y are the fractional nonlinearities specified for the X and Y inputs

EXAMPLE: For Model 429A, $\epsilon_x = 0.5\%$, $\epsilon_y = 0.3\%$. What maximum error can one expect for x = 5V, y = 1V, providing the offset is zeroed out? Can one get less by interchanging inputs?

1. Nominal output is XY/10 = (5)(1)/10 = 500mV
2. Expected error is (5) (0.5%) + (1) (0.3%) = 28mV, 5.6% of output (0.28% of F.S.)
3. Interchanging inputs (1) (0.5%) + (5) (0.3%) = 20mV, 4.0% of output (0.20% of F.S.)

Compare this with the overly conservative error predicted by the overall 1% of full scale specification: 100mV, or 20% of output.

FREQUENCY RELATED SPECIFICATIONS

Accuracy, and its components, feedthrough, linearity, gain, (and phase shift) are frequency dependent. Feedthrough is constant up to 100kHz for the Y input, and up to 400kHz for the X input. Beyond these frequencies it rises at approximately a 6dB/octave rate due to distributed capacitive coupling. A plot of typical feedthrough vs. frequency is shown in Figure 1. For this measurement one input is driven with a 20V p-p sine wave while the other input is grounded and the feedthrough is measured at the output. This error will decrease roughly in proportion to the input signal, and will also vary with temperature (about 0.01%/°C of the nonzero input). Low frequency feedthrough error can be further reduced from the internally trimmed limits by the use of optional external potentiometers.

Non-linearity likewise increases with frequency at a 6dB/octave rate above the break frequency. With the Y input driven

(continued on page 3)

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS (typical @ +25°C and ±15VDC unless otherwise noted)

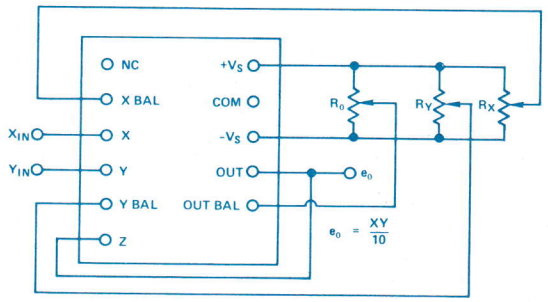
MODEL	429A	429B
MULTIPLICATION CHARACTERISTICS		
Output Function	XY/10	*
Error, with Internal Trim	±1% max	±0.5% max
Error, with External Trim	±0.7%	±0.3%
Avg vs. Temp	±0.05%/°C	±0.04%/°C max
Avg vs. Supply	±0.05%/%	*
SCALE FACTOR		
Initial Error	0.5%	0.25%
Avg vs. Temp	0.03%/°C	0.02%/°C
Avg vs. Supply	0.03%/%	*
OUTPUT OFFSET		
Initial at +25°C	±20mV max	±10mV max
Avg vs. Temp	±2mV/°C	±1mV/°C max
Avg vs. Supply	±1mV/%	*
NON-LINEARITY		
X Input		
(X = 20V p-p 50Hz, Y = ±10V)	0.5% max	0.2% max
Y Input		
(Y = 20V p-p 50Hz, X = ±10V)	0.3% max	0.2% max
FEEDTHROUGH		
X = 0, Y = 20V p-p, 50Hz	50mV p-p, max	20mV p-p, max
With External Trim	16mV p-p	10mV p-p
Y = 0, X = 20V p-p, 50Hz	100mV p-p, max	30mV p-p, max
With External Trim	50mV p-p	20mV p-p
BANDWIDTH		
-3dB	10MHz	*
Full Power Response	2MHz min	*
Slew Rate	120V/μsec min	*
1% Amplitude Error	300kHz min	*
1% Vector Error (0.57°)	50kHz min	*
Differential Phase Shift ($\theta_x - \theta_y$)	1° @ 1MHz	*
Small Signal Rise Time 10-90%	40nsec	*
Small Settling to ±1% (±10V step)	500nsec	*
Overload Recovery	0.2μsec	*
OUTPUT NOISE		
5Hz to 10kHz	0.6mV rms	*
5Hz to 10MHz	3.0mV rms	*
OUTPUT CHARACTERISTICS		
Voltage, 1kΩ load	±11V min	*
Current	±11mA min	*
Load Capacitance	0.01μF max	*
INPUT RESISTANCE		
X Input	10kΩ±5%	*
Y Input	11kΩ±2%	*
Z Input	27kΩ±10%	*
INPUT BIAS CURRENT		
Input X, Y, Z	±100nA	*
Z	±20μA	*
MAXIMUM INPUT VOLTAGE		
For Rated Accuracy	±10.5V	*
Maximum Safe	±16V	*
WARM UP		
To Rated Specifications	1 second	*
POWER SUPPLY[1]		
Rated Performance	±(14.8 to 15.3)VDC	*
Operating	±(14 to 16)VDC	*
Quiescent Current	±12mA	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Weight	2 oz.	*
Socket	AC1023 @ $4.50 (1-9)	*
Case Dimensions	1.5" x 1.5" x 0.62"	*
PRICE		
(1-9)	$117.75	$152.25
(10-24)	$112.50	$141.75

*Specifications same as Model 429A.
[1] Recommend Model 904 available from Analog Devices @ $41.00 (1-9).
Specifications subject to change without notice.

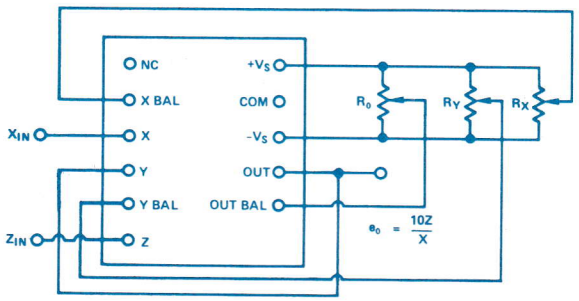
PIN CONNECTIONS

Bottom View Shown in all Cases.
Optional Trim Pots
Shown are not Required
for Rated Accuracy.

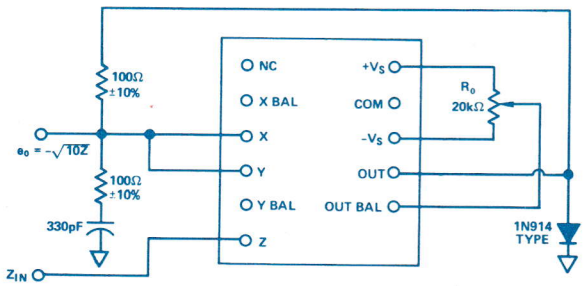
MULTIPLY MODE



DIVIDE MODE



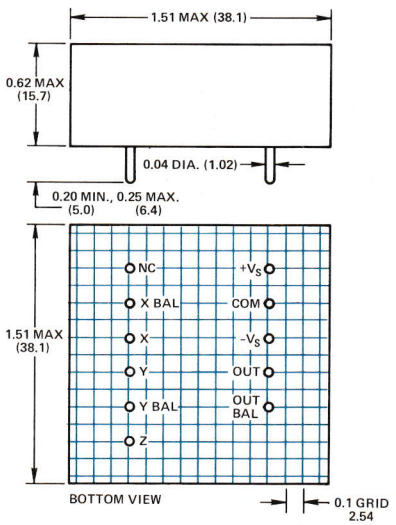
SQUARE ROOT MODE



All trim pots 20kΩ; PN79PR20k $4.75 (1-9).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



(continued from page 1)

at 10V p-p, and the X input anywhere between ±10VDC, the break frequency is 25kHz. For corresponding X input conditions, the break occurs at 60kHz. Figure 1 is a plot of the typical feedthrough vs frequency for the Model 429.

Gain and input to output phase shift for the Model 429 are shown in Figure 2. Naturally, no multiplier will maintain accuracy at frequencies approaching the small signal bandwidth. For the Model 429, the 1% amplitude error will occur at 500kHz. If input to output phase shift is a criterion, then the 1% "vector" error occurs at 50kHz.

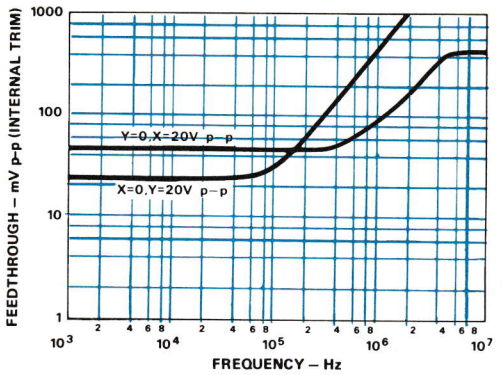


Figure 1. Feedthrough vs Frequency

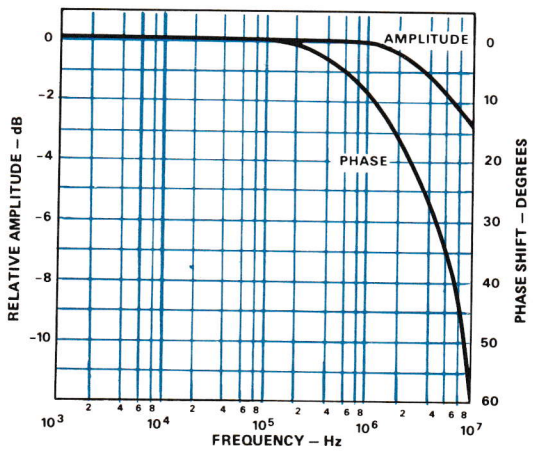


Figure 2. Typical Amplitude and Phase vs Frequency

OPTIONAL TRIM – MULTIPLY MODE

As shipped, the multiplier meets its listed specifications without use of any external trim potentiometers. Terminals are provided for optional feedthrough and offset adjustments. Using these adjustments overall static multiplication error may be reduced to only 0.2%. The 20kΩ trim potentiometers should be connected across the ± supply voltage terminals with the arm of each potentiometer connected to the desired balance terminal (see Page 2).

ADJUSTMENT PROCEDURE FOR OFFSET

1. Jumper X input and Y input to ground.
2. Adjust R_0 for an output of zero volts.
3. Remove jumper from X and Y inputs.

ADJUSTMENT PROCEDURE FOR FEEDTHROUGH

1. Jumper Y input to ground and apply 20 VPP at 1kHz to X input.
2. Adjust R_Y for minimum output voltage.
3. Remove jumper from Y input.
4. Jumper X input to ground and apply 20 VPP at 1kHz to Y input.
5. Adjust R_X for minimum output voltage.
6. Remove jumper from X terminal.

DIVISION

The high bandwidth and excellent linearity of model 429 allows it to be used in divider applications achieving high performance in the DC to 8MHz region. Restrictions imposed on divide operation, and the contributions of error terms are illustrated in the error analysis below.

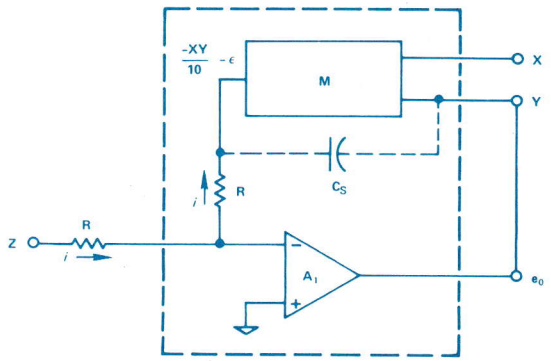


Figure 3. Divider Circuit

Shown in Figure 3 is a typical multiplier/divider which has been connected for divide operation by inserting the multiplier cell, M, in the op amp's feedback loop. Errors associated with the op amp, A_1, are incorporated in ϵ, which represents all errors. In order to insure negative feedback, the X input range is restricted to negative values.

Summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{\frac{XY}{10} + \epsilon}{R} .$$

Solving for Y, which is also ϵ_0:

$$Y = \frac{10\,(Z - \epsilon)}{X}$$

or,

$$\epsilon_0 = \frac{10Z}{X} - \frac{10\epsilon}{X} .$$

And now breaking ϵ into its constituents

$$\epsilon_0 = \underbrace{\frac{10Z}{X}}_{\text{ideal divider}} - \underbrace{\frac{10E_{NV}}{X}}_{\text{noise error}} - \underbrace{\frac{10E_{OS}}{X}}_{\text{offset error}} - \underbrace{\frac{10E_{OS}/^{\circ}C}{X}}_{\text{offset drift error}} - \underbrace{\frac{10E_{NLX}}{X}}_{\text{X non-linearity error}} - \underbrace{\frac{10E_{NLY}}{X}}_{\text{Y non-linearity error}}$$

These errors can be broken down into two categories, static errors and signal dependent errors. All of the static errors associated with the divide mode are inversely proportional to the denominator signal level. The signal dependent errors are the X and Y nonlinearities. For model 429B nonlinearity errors are 0.2% for both the X and Y inputs. Substituting these values in the error terms yields:

$$- \frac{10\,(0.2\%)\,X}{X} - \frac{10\,(0.2\%)\,Y}{X}$$

The importance of using the terminal with largest nonlinearity for the denominator is revealed by the above expression. Effects of X nonlinearity are virtually independent of signal level and may be trimmed out. Nonlinearities of Y typically contribute 200mV for X = Z = 1V i.e., (10 [0.2%] 10V) = 200mV. This error can be reduced if external trims are used to optimize divider performance.

Bandwidth is also degraded with a decrease in denominator level, due to the increase in system gain;

i.e.) for X = Z = 1V, ϵ_0 = 10V

$$\text{and} \quad \frac{\epsilon_0}{Z} = \frac{10}{1} = 10$$

Since the gain bandwidth product is constant, a bandwidth of 1/10 of that obtained for full scale denominator levels will be obtained for division at 1V levels.

For other denominator levels, bandwidth is determined by:

$$\text{B. W.} = \frac{\text{Denominator Level}}{\text{Full Scale Denominator}} \text{ x (Multiplier B.W.) x K}$$

where K is a constant having a value less than unity. It is introduced due to a combination of stray capacitance paralleling the multiplier cell and effects of feedthrough. For model 429

$$\text{B.W.} = \left(\frac{X}{10}\right) 8\text{MHz}$$

Before selecting a multiplier/divider for divide applications, errors resulting from the lowest anticipated denominator signal should be considered. After such considerations have been made, one can further appreciate the importance of starting with an accurate, high speed multiplier such as model 429. It is also highly recommended that the optional trim procedure for division be performed.

OPTIONAL TRIMMING – DIVIDE MODE

Connections are made as shown on page 2.

The suggested trim procedure is (starting with centered adjust adjustments):

*1. With Z = 0, trim R_0 to hold output constant, as X is varied from -10V toward -1.0V.
2. With Z = 0, trim R_Y for zero at X = -10V.
3. With Z = X and/or Z = -X, trim R_X for minimum worst-case variation as X is varied from -10V to -1.0V.
4. Repeat 1 and 2 if step 3 required large initial adjustment.

*For best accuracy X should be allowed to vary from -10V to lowest expected denominator.

SQUARE ROOTING

When connected as shown on page 2, the model 429 will provide the square root of Z_{IN}.

By summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{XY}{10R} + \frac{\epsilon}{R} = \frac{Y^2}{10R} + \frac{\epsilon}{R}$$

where ϵ represents all errors associated with the multiplier. Solving for the output voltage, Y.

$$\epsilon_0 = \pm \sqrt{10\,(Z - \epsilon)}$$

There are two values of ϵ_0 for every value of Z. However, only negative values of ϵ_0 will provide the negative feedback necessary for circuit stability. To restrict the output from going positive, a diode is connected as shown on page 2. The output is then:

$$\epsilon_0 = -\sqrt{10\,(Z - \epsilon)}$$

Errors, ϵ, associated with the multiplier, are inside the square root and consequently their effect, for large values of Z, is reduced. The reason for the improved performance can be seen by inspecting the circuit. The output is fed back to both the X and Z terminals, resulting in twice the feedback as would be obtained for the divide mode. An alternative method of considering error performance is to consider errors as being at the Z terminal. By differentiating the ideal transfer function with respect to Z, errors for various values of Z may be determined:

$$\frac{de_0}{dZ} = \frac{d}{dZ}\sqrt{10Z} = \tfrac{1}{2}\sqrt{\frac{10}{Z}}$$

The factor of ½ has the advantage of reducing errors by a factor of 2 for Z = 10, but also introduces the potential problem of instability. Since the feedback gain is the reciprocal of the forward gain, the slope of the forward gain is 2. Additional phase margin is required to support the increased gain in the feedback path. Model 429 is optimized for phase margin in the multiply and divide modes producing minimum vector errors at high frequencies. To avoid the potential problem of instability, the RC network shown on page 2 is recommended. This network restricts the bandwidth and guarantees stability for all positive values of Z.

OPTIONAL ADJUSTMENT PROCEDURE – SQUARE ROOT

1. Apply a voltage to the Z terminal equal to the lowest anticipated input voltage.
2. Adjust R_0 such that $e_0 = \sqrt{10Z}$, where Z_1 is the voltage applied in step 1.

DIVISION SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	10(Z)/X
Numerator Range	±10V
Denominator Range, 1% Accuracy	-1 to -10V
Denominator Range, 5% Accuracy	-0.2V to -10V
Bandwidth Formula, (Hz, -3dB)	(8MHz)(X)/10

SQUARE ROOTING SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	$-\sqrt{10(Z)}$
Dynamic Range	1000 to 1 (+0.010V ≤Z≤+10V)
Accuracy (% of Full Scale)	0.5%
Bandwidth Formula, (Hz, -3dB)	$(5\text{MHz})\sqrt{\lvert X\rvert/10}$

Table 1. Division & Square Rooting Specifications

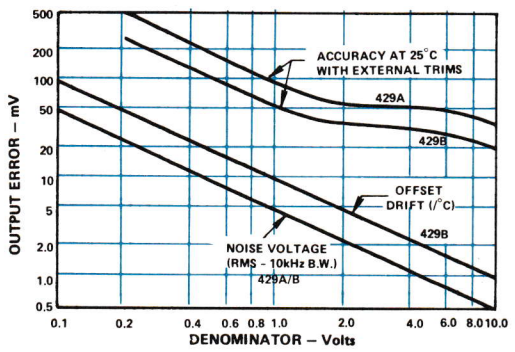


Figure 3. Typical Error Performance of Model 429 in Divide Mode for Worst Case of $|e_0| = 10V$.

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FEATURES

- 15 nsec PROPAGATION DELAY
- COMPLEMENTARY OUTPUT GATES
- TTL OR ECL COMPATIBLE OUTPUTS
- WIDE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE

APPLICATIONS

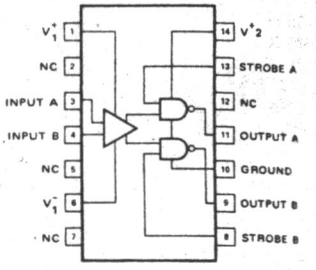
A/D CONVERSION
ECL TO TTL INTERFACE
TTL TO ECL INTERFACE
MEMORY SENSING
OPTICAL DATA COUPLING

ABSOLUTE MAXIMUM RATINGS

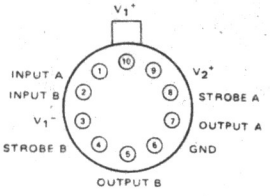
Positive Supply Voltage (V1+)	+15 volts
Negative Supply Voltage (V1−)	−15 volts
Gate Supply Voltage (V2+)	+7 volts
Output Voltage	+15 volts
Differential Input Voltage	±5 volts
Input Common Mode Voltage	±6 volts
Power Dissipation	600mW
Operating Temperature Range	
NE527	0°C to +70°C
SE527	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PIN CONFIGURATION

A PACKAGE



K PACKAGE

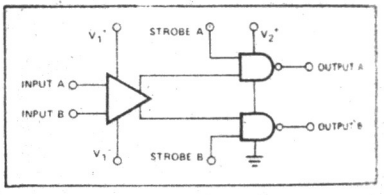


ELECTRICAL CHARACTERISTICS (T_A + 25°C)

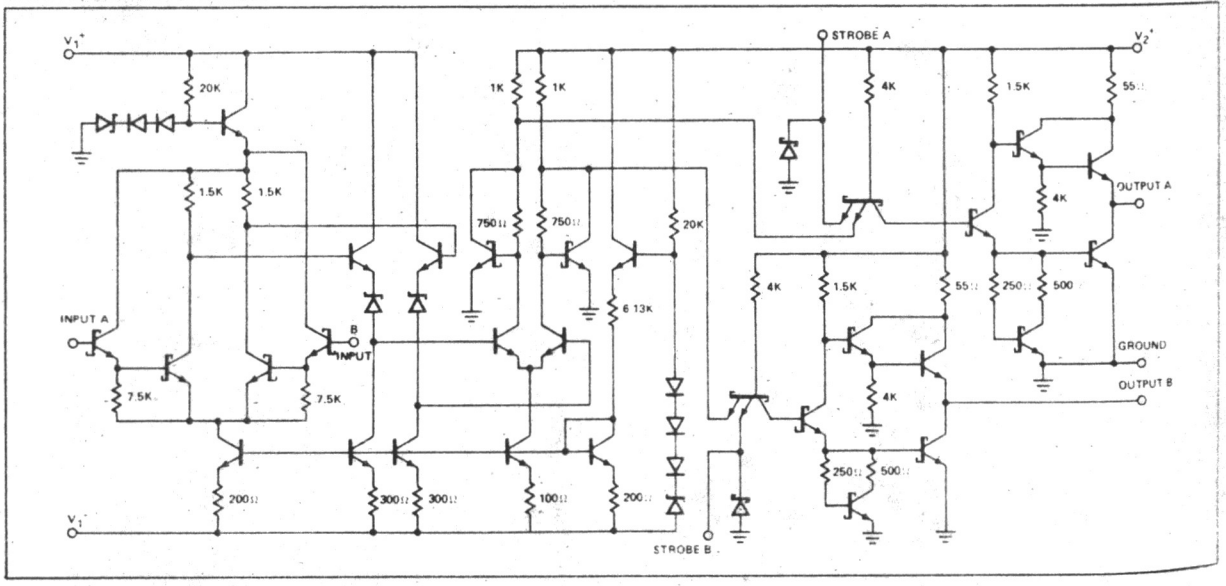
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Input Impedance	f = 1kHz		500		KΩ
Transient Response	V_{in} = 50mV overdrive				
Propagation Delay Time					
t_{PLH}			16	26	ns
t_{PHL}			14	24	ns
Delay between Output A and B			2	5	ns
Strobe Delay Time					
t_{on} Turn-on time			6		ns
t_{off} Turn-off time			6		ns

Parameters are guaranteed over the temperature range unless otherwise noted.

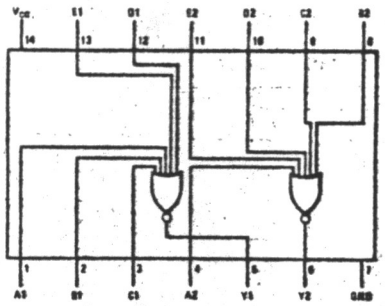
BLOCK DIAGRAM



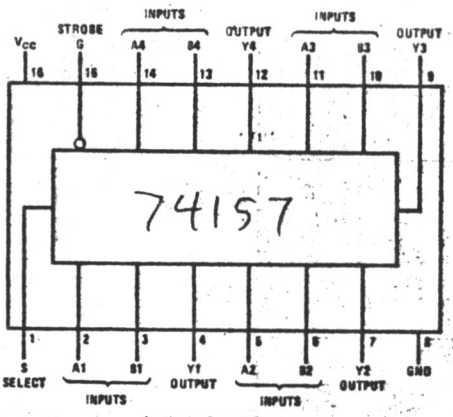
EQUIVALENT CIRCUIT



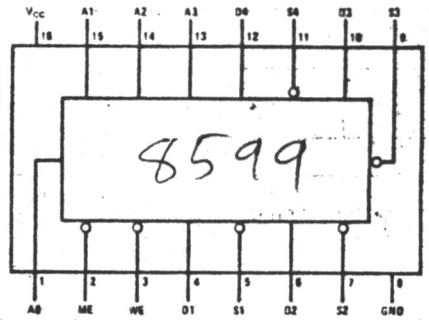
DIGITAL



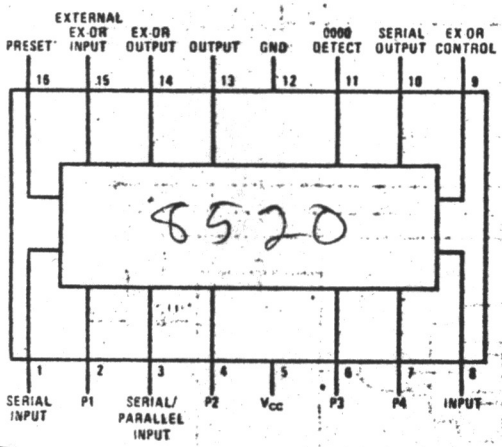
74S260(N)



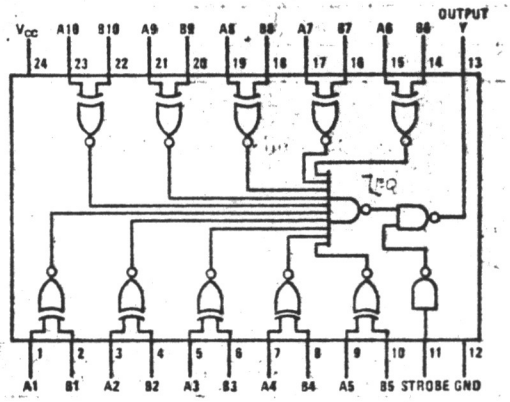
Low level at S selects A inputs
High level at S selects B inputs



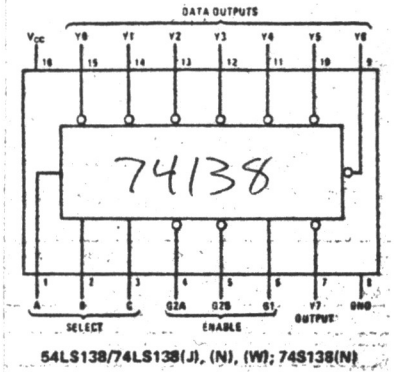
7599(J); 8599(J), (N)



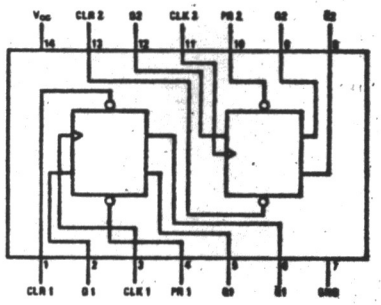
7520(J), (W); 8520(J), (N), (W)



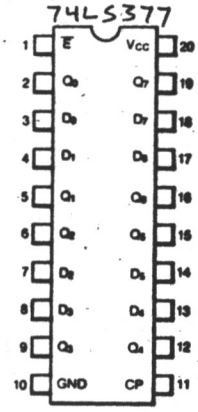
7130(J), (F); 8130(J), (N), (F)

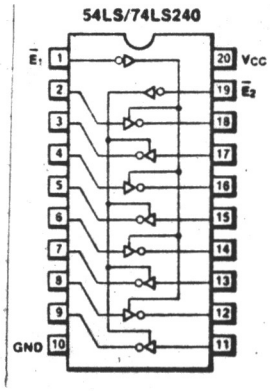


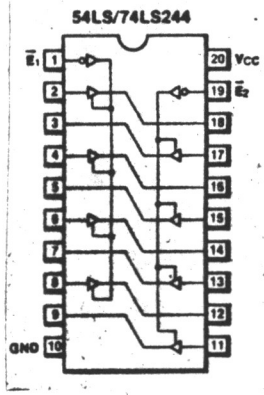
54LS138/74LS138(J), (N), (W); 74S138(N)

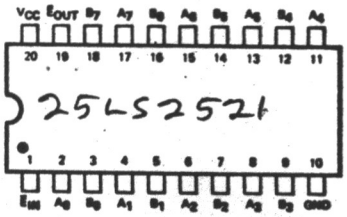


5474/7474(J),(N); 54H74/74H74(J),(N); 54L74/74L74(J),(N); 54LS74/74LS74(J),(N),(W); 74S74(N)

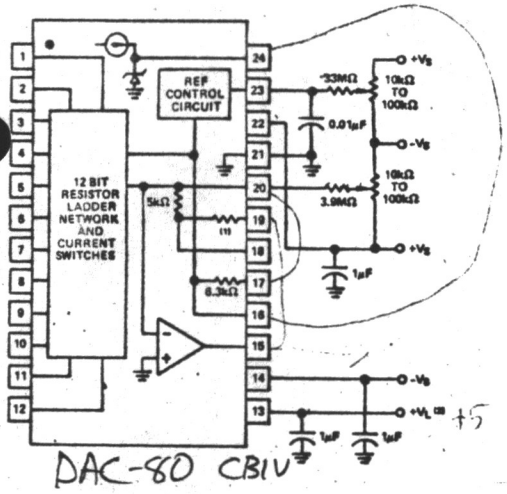






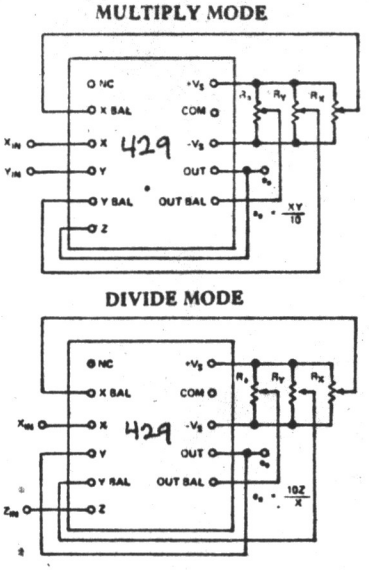


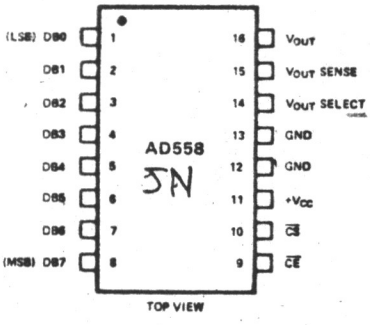
ANALOG

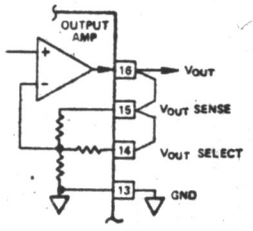


Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

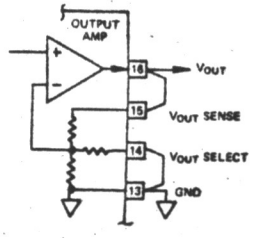
Table III. Output Voltage Range Connections-Voltage Model AD DAC80



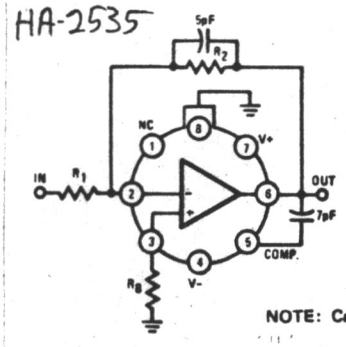




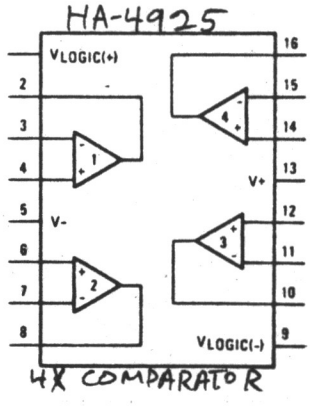
a. 0V to 2.56V Output Range

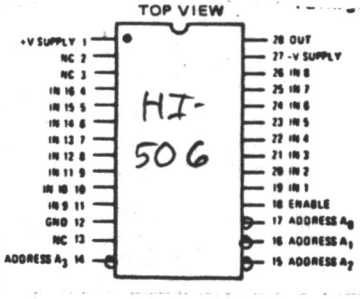


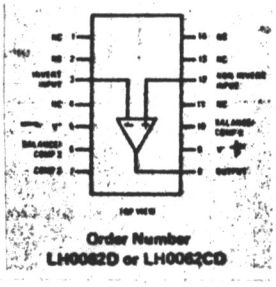
b. 0V to 10V Output Range

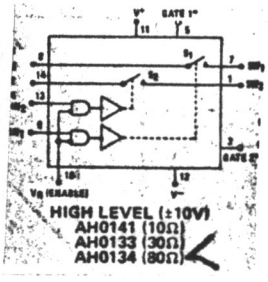


NOTE: Case









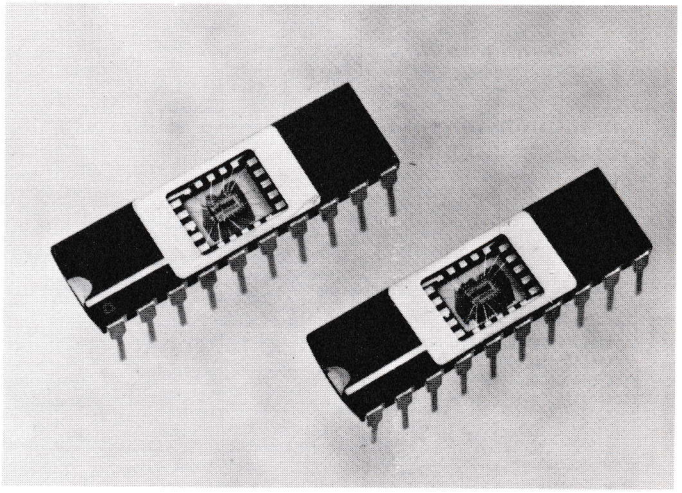
ANALOG DEVICES

CMOS 12-Bit Buffered Multiplying DAC

AD7545

FEATURES

- 12-Bit Resolution
- Low Gain T.C.: 2ppm/°C typ
- Fast TTL Compatible Data Latches
- Single +5V to +15V Supply
- Small 20-Pin 0.3" DIP
- Latch Free (Schottky Protection Diode Not Required)
- Low Cost
- Ideal for Battery Operated Equipment



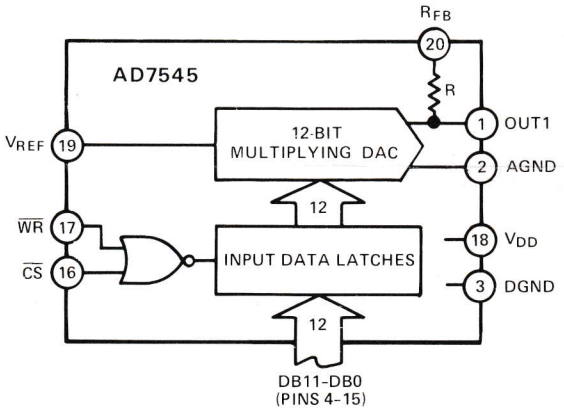
GENERAL DESCRIPTION

The AD7545 is a monolithic 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

The AD7545 can be used with any supply voltage from +5V to +15V. With CMOS logic levels at the inputs the device dissipates less than 0.5mW for V_{DD} = +5V.

AD7545 FUNCTIONAL DIAGRAM

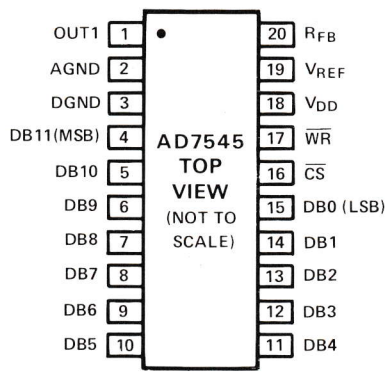


ORDERING INFORMATION

Relative Accuracy	Maximum Gain Error T_A = +25°C V_{DD} = +5V	Temperature Range and Package[1] Plastic[2] 0 to +70°C	Cerdip[3,4] -25°C to +85°C	Ceramic[3] -55°C to +125°C
±2LSB	±20LSB	AD7545JN	AD7545AQ	AD7545SD
±1LSB	±10LSB	AD7545KN	AD7545BQ	AD7545TD
±1/2LSB	±5LSB	AD7545LN	AD7545CQ	AD7545UD
±1/2LSB	±1LSB	AD7545GLN	AD7545GCQ	AD7545GUD

NOTES:
[1] Analog Devices is offering the AD7545 in chip carriers, for further information contact the factory.
[2] Plastic encapsulated units will be available by early 1982.
[3] 883B version is available. To order add "/883B" to part number shown.
[4] Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

PIN CONFIGURATION



Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 **TWX: 710/394-6577**
West Coast 714/842-1717 **Mid-West 312/653-5000** **Texas 214/231-5094**

SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified)

Parameter	Version	V_{DD} = +5V Limits T_A = +25°C	T_{min}, T_{max} [1]	V_{DD} = +15V Limits T_A = +25°C	T_{min}, T_{max} [1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB max	
	K, B, T	±1	±1	±1	±1	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB max	10-Bit Monotonic T_{min} to T_{max}
	K, B, T	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	L, C, U	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	GL, GC, GU	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
Gain Error (Using Internal RFB)[2]	J, A, S	±20	±20	±25	±25	LSB max	DAC Register Loaded with
	K, B, T	±10	±10	±15	±15	LSB max	1111 1111 1111
	L, C, U	±5	±6	±10	±10	LSB max	Gain Error is Adjustable Using
	GL, GC, GU	±1	±2	±6	±7	LSB max	the Circuits of Figures 4, 5 and 6
Gain Temperature Coefficient[3] ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C max	Typical Value is 2ppm/°C for V_{DD} = +5V
DC Supply Rejection[3] ΔGain/ΔV_{DD}	All	0.015	0.03	0.01	0.02	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	J, K, L, GL	10	50	10	50	nA max	DB0–DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA max	
	S, T, U, GU	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Propagation Delay[3] (from Digital Input Change to 90% of final Analog Output)	All	300	–	250	–	ns max	OUT1 LOAD = 100Ω C_{EXT} = 13pF[4]
Glitch Energy	All	400	–	250	–	nV sec typ	V_{REF} = AGND
AC Feedthrough[5] At I_{OUT1}	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sine Wave:
REFERENCE INPUT							
Input Resistance	All	7	7	7	7	kΩ min	Input Resistance TC = –300ppm/°C max
(Pin 19 to GND)		25	25	25	25	kΩ max	Typical Input Resistance = 11kΩ
ANALOG OUTPUTS							
Output Capacitance[3]							
C_{OUT1}	All	70	70	70	70	pF max	DB0–DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	200	200	200	200	pF max	DB0–DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[6] I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[3]							
DB0–DB11	All	5	5	5	5	pF max	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF max	V_{IN} = 0
SWITCHING CHARACTERISTICS[7]							
Chip Select to Write Setup Time	All	280	380	180	200	ns min	See Timing Diagram on Page 3
t_{CS}		200	270	120	150	ns typ	
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	250	400	160	240	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns typ	
Data Setup Time	All	140	210	90	120	ns min	
t_{DS}		100	150	60	80	ns typ	
Data Hold Time t_{DH}	All	10	10	10	10	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	μA typ	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows: JN, KN, LN, GLN: 0 to +70°C; AQ, BQ, CQ, GCQ: –25°C to +85°C; ST, TD, UD, GUD: –55°C to +125°C

[2] This includes the effect of 5ppm max gain TC.

[3] Guaranteed but not tested.

[4] DB0–DB11 = 0V to V_{DD} or V_{DD} to 0V.

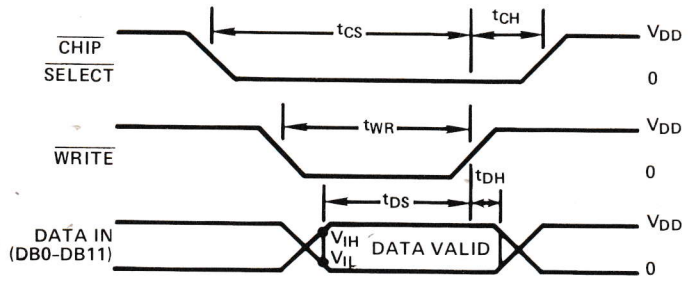
[5] Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

[6] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[7] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $V_{IH} + V_{IL}/2$.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . -0.3V, +17V
Digital Input Voltage to DGND . . . . . -0.3V, V_{DD}
V_{RFB}, V_{REF} to DGND . . . . . ±25V
V_{PIN1} to DGND . . . . . -0.3V, V_{DD}
AGND to DGND . . . . . -0.3V, V_{DD}
Power Dissipation (Any Package) to 75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (JN, KN, LN, GLN) Grades . . . . . 0 to +70°C
Industrial (AQ, BQ, CQ, GCQ) Grades . . . . -25°C to +85°C
Military (SD, TD, UD, GUD) Grades . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: The amount by which the D/A converter transfer function differs from the ideal transfer function after the zero and full scale points have been adjusted. This is an end point linearity measurement.

DIFFERENTIAL NONLINEARITY: The difference between the measured change and the ideal change between any two adjacent codes. If a device has a differential nonlinearity of less than 1LSB then it will be monotonic, i.e., the output will always increase for an increase in digital code applied to the D/A converter.

PROPAGATION DELAY: This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reached 90% of its final value.

GLITCH ENERGY: This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVsecs and is measured with V_{REF} = AGND and an ADLH0032CG as the output op amp, C1 (phase compensation) = 33pF.

PRICES — $ (100s)

AD7545JN	8.00	AD7545LN	11.45
AD7545AQ	9.50	AD7545CQ	12.95
AD7545SD	27.00	AD7545UD	38.85
AD7545KN	10.45	AD7545GLN	16.75
AD7545BQ	11.95	AD7545GCQ	19.20
AD7545TD	35.85	AD7545GUD	57.60

CIRCUIT INFORMATION – D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of the AD7545 and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

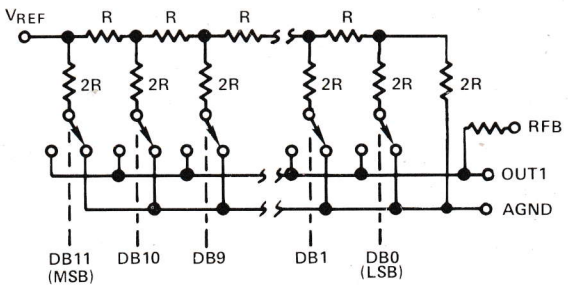


Figure 1. Simplified D/A Circuit of AD7545

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

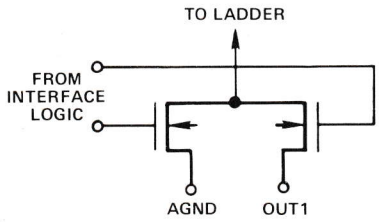


Figure 2. N-Channel Current Steering Switch

CIRCUIT INFORMATION–DIGITAL SECTION

Figure 3 shows the digital structure for one bit.

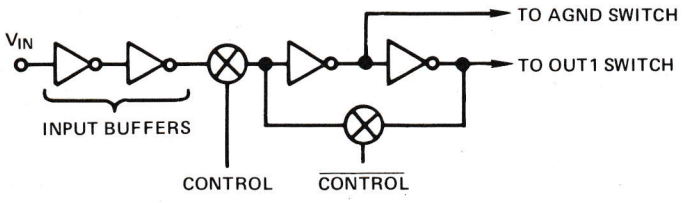


Figure 3. Digital Input Structure

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range $5 \leqslant V_{DD} \leqslant 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. The "G" versions (AD7545GLN, AD7545GCQ, AD7545GUD) have a guaranteed maximum gain error of ±1LSB at +25°C (V_{DD} = +5V) and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that all the circuits of Figures 4, 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leqslant V_{IN} \leqslant +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 4.

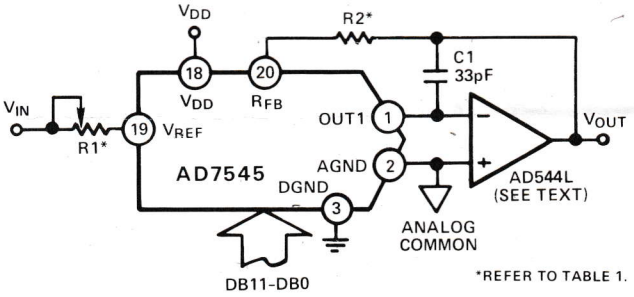


Figure 4. Unipolar Binary Operation

TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/TD	GLN/GCQ/GUD
R1	500Ω	100Ω	50Ω	10Ω
R2	100Ω	47Ω	22Ω	4.7Ω

Table 1. Recommended Trim Resistor Values vs. Grades

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table 2. Unipolar Binary Code Table for Circuit of Figure 4

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software

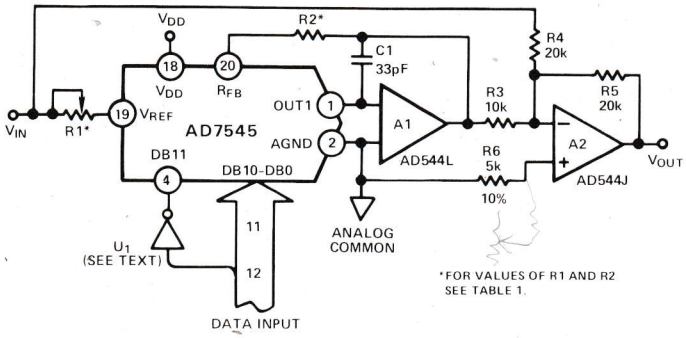


Figure 5. Bipolar Operation (2's Complement Code)

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table 3. 2's Complement Code Table for Circuit of Figure 5

using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wirewound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for

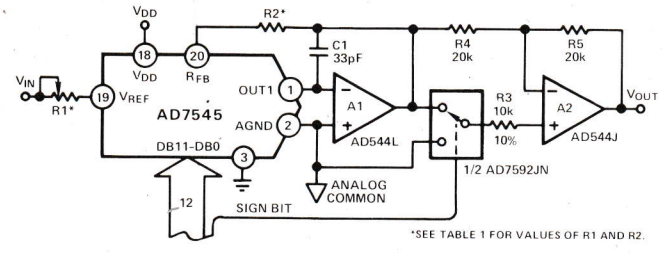


Figure 6. 12-Bit Plus Sign Magnitude D/A Converter

the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

Sign Bit	Binary Numbers in DAC Register			Analog Output
0	1111	1111	1111	$+V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	$-V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$

Note: Sign bit of "0" connects R3 to GND.

Table 4. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6.

APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifer. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5 volts. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

SINGLE SUPPLY OPERATION

The ladder termination resistor of the AD7545 (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT 1 and AGND may be biased at any voltage between DGND and V_{DD}. OUT1 and AGND should never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow which will damage the device. (The AD7545 is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices.)

Figure 7 shows the AD7545 connected in a voltage switching mode. OUT1 is connected to the reference voltage and AGND is connected to DGND. The D/A converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in this circuit.

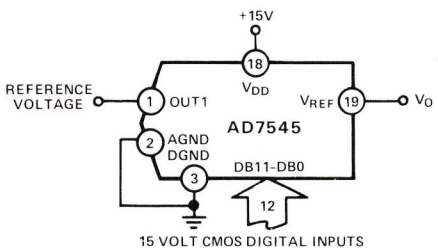


Figure 7. Single Supply Operation Using Voltage Switching Mode

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltages at OUT1 and AGND should remain within 2.5 volts of each other, for a V_{DD} of 15 volts. If V_{DD} is reduced from 15V or the differential voltage between OUT1 and AGND is increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. If the output voltage is required to be offset from ground by some value, then OUT1 and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset.

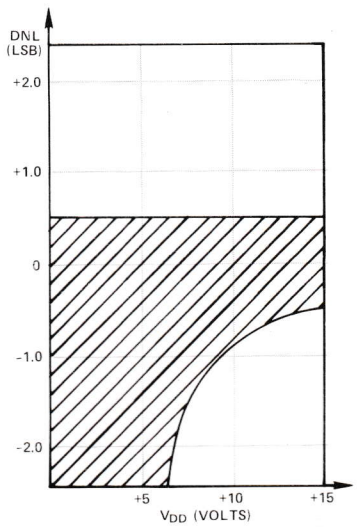


Figure 8. Differential Nonlinearity vs. V_{DD} for Figure 7 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

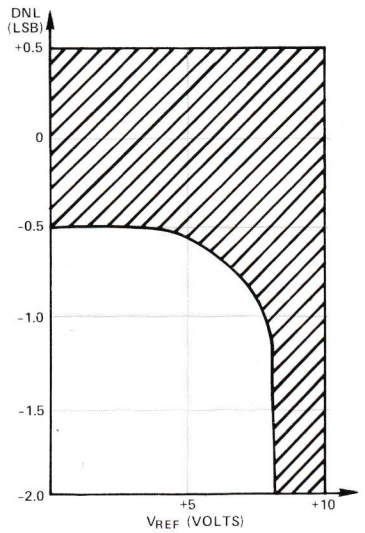


Figure 9. Differential Nonlinearity vs. Reference Voltage for Figure 7 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

The circuits of Figures 4, 5 and 6 can all be converted to single supply operation by biasing AGND to some voltage between V_{DD} and DGND. Figure 10 shows the 2's Complement Bipolar circuit of Figure 5 modified to give a range from +2V to +8V about a "pseudo-analog ground" of 5V. This voltage range would allow operation from a single V_{DD} of +10V to +15V. The AD584 pin-programmable reference fixes AGND at +5V. V_{IN} is set at +2V by means of the series resistors R1 and R2. There is no need to buffer the V_{REF} input to the AD7545 with an amplifier because the input impedance of the D/A converter is constant. Note, however, that since the temperature coefficient of the D/A reference input resistance is typically -300ppm/°C, applications which experience wide temperature variations may require a buffer amplifier to generate the +2.0V at the AD7545 V_{REF} pin. Other output voltage ranges can be obtained by changing R4 to shift the zero point and (R1 + R2) to change the slope, or gain of the D/A transfer function. V_{DD} must be kept at least 5V above OUT1 to ensure that linearity is preserved.

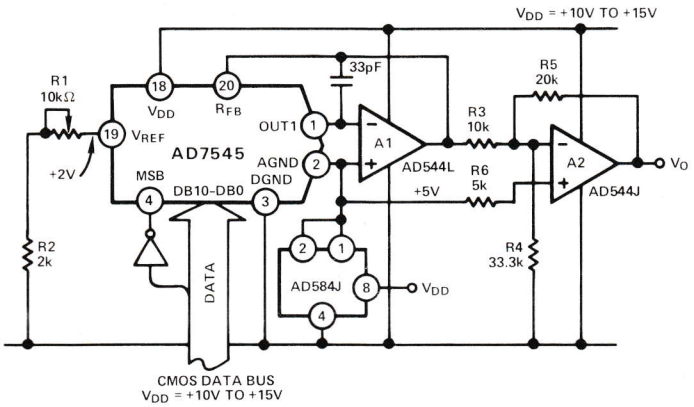


Figure 10. Single Supply "Bipolar" 2's Complement D/A Converter

MICROPROCESSOR INTERFACING OF THE AD7545

The AD7545 can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 11. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

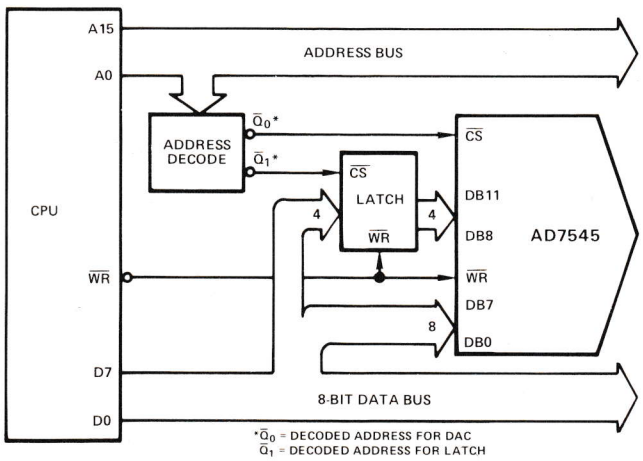


Figure 11. 8-Bit Processor to AD7545 Interface

Figure 12 shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower

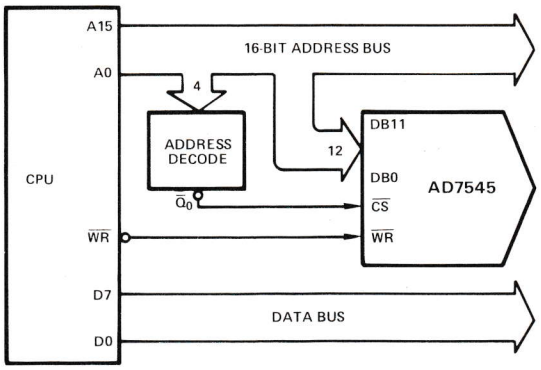


Figure 12. Connecting the AD7545 to 8-Bit Processors via the Address Bus

address lines of the processor address bus to supply data to the DAC, thus each AD7545 connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

Application Guide to CMOS Multiplying D/A converters available from Analog Devices, Publication Number G479.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACS – Application Note, Publication Number E630–10–6/81 available from Analog Devices.

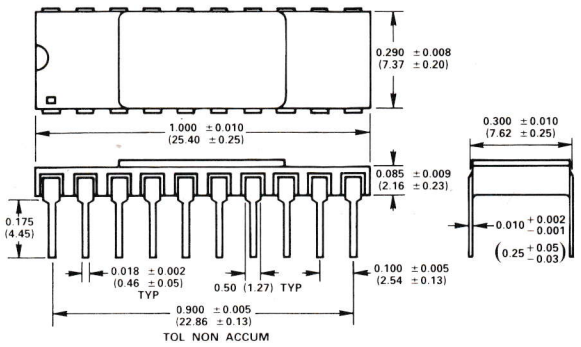
Analog-Digital Conversion Notes – available from Analog Devices, price $5.95.

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

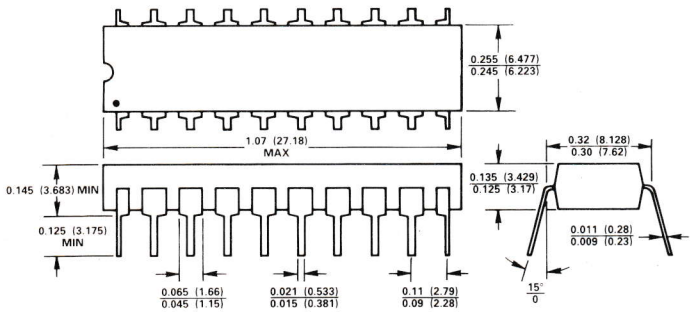
(Dimensions shown in inches and (mm).

20-PIN CERAMIC DIP (SUFFIX D)



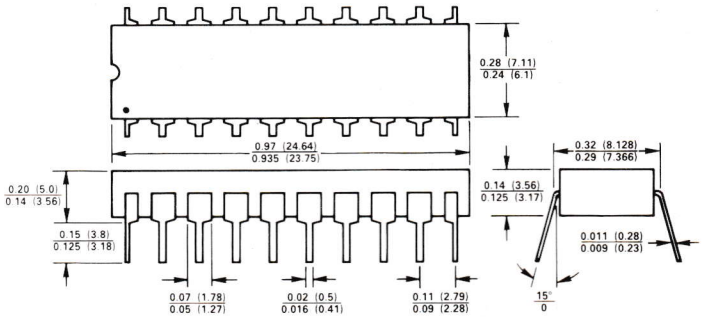
LEAD NUMBER 1 IDENTIFIED BY DOT OR NOTCH.
LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

20-PIN PLASTIC DIP (SUFFIX N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

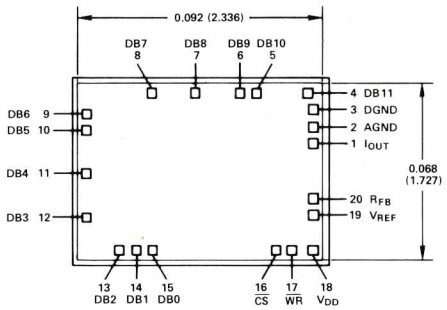
20-PIN CERDIP (SUFFIX Q)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

BONDING DIAGRAM

Dimensions shown in inches and (mm).



PADS ARE 0.004" × 0.004" (0.102 × 0.102)mm.
TO MINIMIZE ESD HAZARD BOND DGND FIRST.

C670-9-10/81

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